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PROCESS VARIABLE DEPENDENCE AND INTERRELATIONSHIP BETWEEN AVALANCHE CHARGE INJECTION AND RADIATION INDUCED CARRIER TRAPPING IN THERMAL OXIDES

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Characterization of the process dependence of avalanche injected electrons and holes in thermally grown silicon dioxide has been carried out. Process parameters investigated include oxidation temperature (800,900,1000, and 1100°C) oxidation ambient (O_2,H_2O and O_2/HCl); oxidation pressure (1,5 and 10 atm), post-oxidation insitu anneal ambient(N_2,Ar), cooling ambient (O_2,N_2,Ar, and H_2O), cooling rates (3 sec, 2 min, and 10 min), pre-metallization anneal in hydrogen, post-metallization anneal ambients (N_2,H_2,N_2/H_2), substrate orientation

((100) and (111)), oxide thickness, polycrystalline silicon field plate deposition and process related radiation exposure (election beam, laser beam, and ion implantation). Results indicate basic differences between the process dependence of electron traps and that of hole traps.

Characteristics of the process dependence of the hole traps are: a minimum for dry O_2 oxides, an increase for N_2 post-oxidation anneals at 1000°C and above, an increase for pre-metallization anneals in H_2, a high density for HCl/O_2 and steam oxides, a minimum for oxides grown on (100) oriented substrates, slightly higher for dry O_2 high pressure oxides, an increase for a polycrystalline silicon deposition step, an increase when exposed to e-beam radiation. minimal when exposed to a laser beam, and an increase for oxides grown on implanted substrates.

Characteristics for the process dependence of electron traps are: a minimum at 1100°C, largest for steam grown oxides, reduced by a post-oxidation anneal in N_2 or Ar at temperatures greater than 800°C, substrate orientation dependence for steam oxides only, an increase for dry O_2 high pressure oxides, a decrease for a polycrystalline silicon field plate deposition step, an increase when exposed to an electron beam and minimal when exposed to a laser beam. Post-metallization anneal ambients were found to have little or no effect on the measured trapping of both holes and electrons. A comparison between radiation induced and avalanche injected carrier trapping has been carried out. The dependence of the density of trapped holes on process parameters, i.e., the case of hole trapping induced by avalanche charge injection or by ionizing radiation, was found to be quite similar. This result was determined to be valid for most of the process parameters investigated. This suggests that the avalanche charge injection technique could be used, along with a suitable test structure, as an "on chip" monitor for radiation hardness.

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PURPOSE

[Begin.]

The primary objective of this program is the investigation of the effects of processing variables on the trapping characteristics of injected charge carriers in thermal silicon dioxide. In addition, the nature and process dependence of avalanche injected trapped charges will be compared to those produced by ionizing radiation in identical oxides. The results obtained from this program should help in the determination of optimum process conditions for minimizing hot carrier trapping in VLSI device structures and in the establishment of accelerated test procedures for the evaluation of radiation trapping properties of thermal oxides.

[to 1473]

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1.0 INTRODUCTION

A joint program has been established between Fairchild Camera and Instrument Corporation and the Naval Research Laboratory, the purpose of which is to characterize the process dependence of the trapping of injected electrons and holes in thermally grown silicon dioxide. The nature of the trapped charge is compared to that produced by ionizing radiation in oxides prepared at the same time and under identical conditions. Results from this program should permit the optimization of the process conditions necessary for VLSI device structures with minimum hot carrier trapping.

MOS test capacitor structures were prepared at Fairchild under controlled conditions. Process parameters under investigation included:

1 – Oxidation ambient (O_2, H_2O, and O_2/HCl)
2 – Oxidation pressure (1, 5, and 10 atm)
3 – Cooling ambient (O_2, N_2, and Ar)
4 – Cooling rate (3 sec, 2 min, and 10 min)
5 – Post-oxidation in-situ anneal (N_2 and Ar)
6 – Polysilicon field plates
7 – Post-metallization anneals (N_2, N_2/H_2, H_2)
8 – Substrate orientation ((100) and (111))
9 – Oxide thickness
10 – Process-related radiation exposure (e-beam lithography, e-beam implant and damage anneal, sputtering, plasma and others).

Carrier injection is achieved by avalanche from a doped substrate ($10^{16} - 10^{17}/cm^3$). The change in flat band voltage as a function of carrier injection time for a constant injection current is monitored by a desktop computer. In some selected cases, quasi-static C-V measurements are performed

at intervals during the avalanche injection. These measurements when coupled with high frequency C-V are used to monitor the generation of interface states during the avalanche injection process.

One-half of all MOS structures were sent to the Naval Research Laboratory where they were exposed to ionizing radiation. The charges induced by the radiation exposure were then measured in order to correlate the results with the avalanche trapping data.

2.0 BACKGROUND

Thermal silicon dioxide has played a key role in the development and growth of the semiconductor industry. Thermally grown silicon dioxide layers have been used for many circuit functions (1) including surface passivation, insulation between layers of metal and/or polycrystalline silicon, and as actual circuit components, as well as for many processing functions such as masking against dopant diffusion and ion implantation.

Thermal SiO_2 layers are formed at temperatures of 700°-1200°C in dry oxygen, wet oxygen, pyrogenic steam, or mixtures thereof at 1 atm and in more recent technological developments at pressures extending up to 25 atm in commercially available systems (2). The growth kinetics of thermal silicon dioxide films have been characterized by a general relationship (3) and the electrical properties of the films are found to be intimately related to the oxidation growth parameters such as oxidation ambient, post-oxidation anneals, and cooling rates.

The presence of charges in an oxide can induce corresponding charges of the opposite polarity in the underlying silicon. These charges can affect many of the characteristics of both MOS and bipolar devices such as junction noise, leakage, and breakdown; leakage or channeling between devices; low current beta; and MOS threshold voltages. In order to more fully understand the effect of processing parameters on the electrical properties of the thermally grown silicon dioxide films, it is necessary to characterize the types of charges present in these films. Four main charge categories have been identified and associated with the SiO_2 films and the Si/SiO_2 interface (4,5). These charges are indicated in Fig. 2-1 and can be described as follows:

N_f – fixed oxide charge, located in the oxide near the Si/SiO_2 interface

N_{it} – interface trapped charge or states, located at the
D_{it} Si/SiO_2 interface and in electrical communication with the silicon

N_m – mobile ionic charge, located throughout the oxide, and generally a positive alkali ion (Na^+, H^+)

N_{ot} – oxide trapped charge, located at the interface and/or the bulk of the SiO_2, made up of electrons or holes trapped by various means in the oxide.

In the above $N \equiv Q/q$ is the effective number of charges at the Si/SiO_2 interface in units of cm^{-2}, and $D_{it} \equiv$ density of interface trapped charge at the Si/SiO_2 interface in units of $cm^{-2}-eV^{-1}$.

Of these four types of charges, N_f and N_{it} are known to be associated with the oxidation process. The oxide fixed charge has been postulated to arise from partially ionized silicon, while the structural type of interface states seem to have a similar origin, possibly trivalent silicon tied to three silicon atoms (4,6,7). Direct relationships between N_f and N_{it} and process variables such as silicon orientation, oxidation temperature, and annealing/cooling conditions have been investigated thoroughly (8-12) and the interdependence of N_f and N_{it} documented (12).

The oxide trapped charges, which include both trapped electrons and holes, have been investigated by various means including internal photoemission (13-15), avalanche injection of the substrate by means of voltage pulses (16-18), avalanche injection by means of p-n junctions (19), optically induced

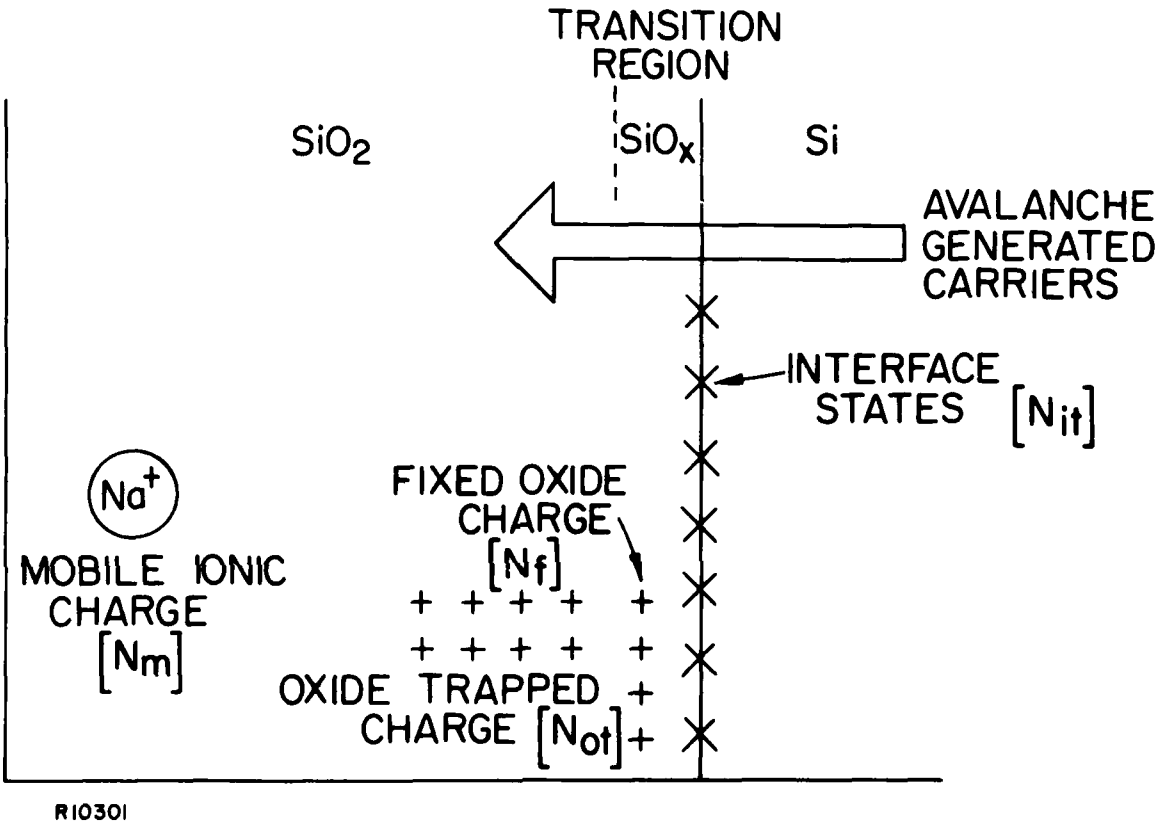

Fig. 2-1. The four types of charges associated with the thermally oxidized silicon structure.

hot electrons from n-channel silicon gate structures (20), forward biased p-n junctions using epitaxial silicon layers (19-21), high electric fields (22), ionizing radiation such as x-rays (23-25), γ-rays (26), VUV light (27-29), and high energy electrons (30). The considerable amount of work carried out dealing with oxide trapped charge is a reflection of the importance attached to understanding both the process dependence and the physical origin of the trapped charge.

The main reason behind the increasing interest in charge trapping in thermal oxides is primarily related to device reliability, particularly in the case of MOS devices. It has been proposed that new processing techniques now being introduced such as sputtering, plasma etching and stripping, electron beam and x-ray lithography, electron and laser beam annealing, as well as established processes such as electron beam metal evaporation and ion implantation through gate oxides (31-33), can produce neutral oxide traps. These traps could, during subsequent irradiation, be a major source of device degradation. A brief summary of the process parameters that can affect carrier trapping in thermal oxides is shown in Fig. 2-2 and includes standard oxidation and annealing processes in addition to the more advanced techniques mentioned.

The selection of optimum process techniques is becoming more critical to advanced device fabrication. Furthermore, new constraints are being imposed by device scaling in the continuing effort to achieve greater packing densities and better performance. Shrinking geometries can lead to increasing electric field intensities which in turn result in hot carrier generation and injection into the oxide. In present devices, sources of hot carriers such as p-n junction avalanche plasmas, channel currents, multiplication currents associated with

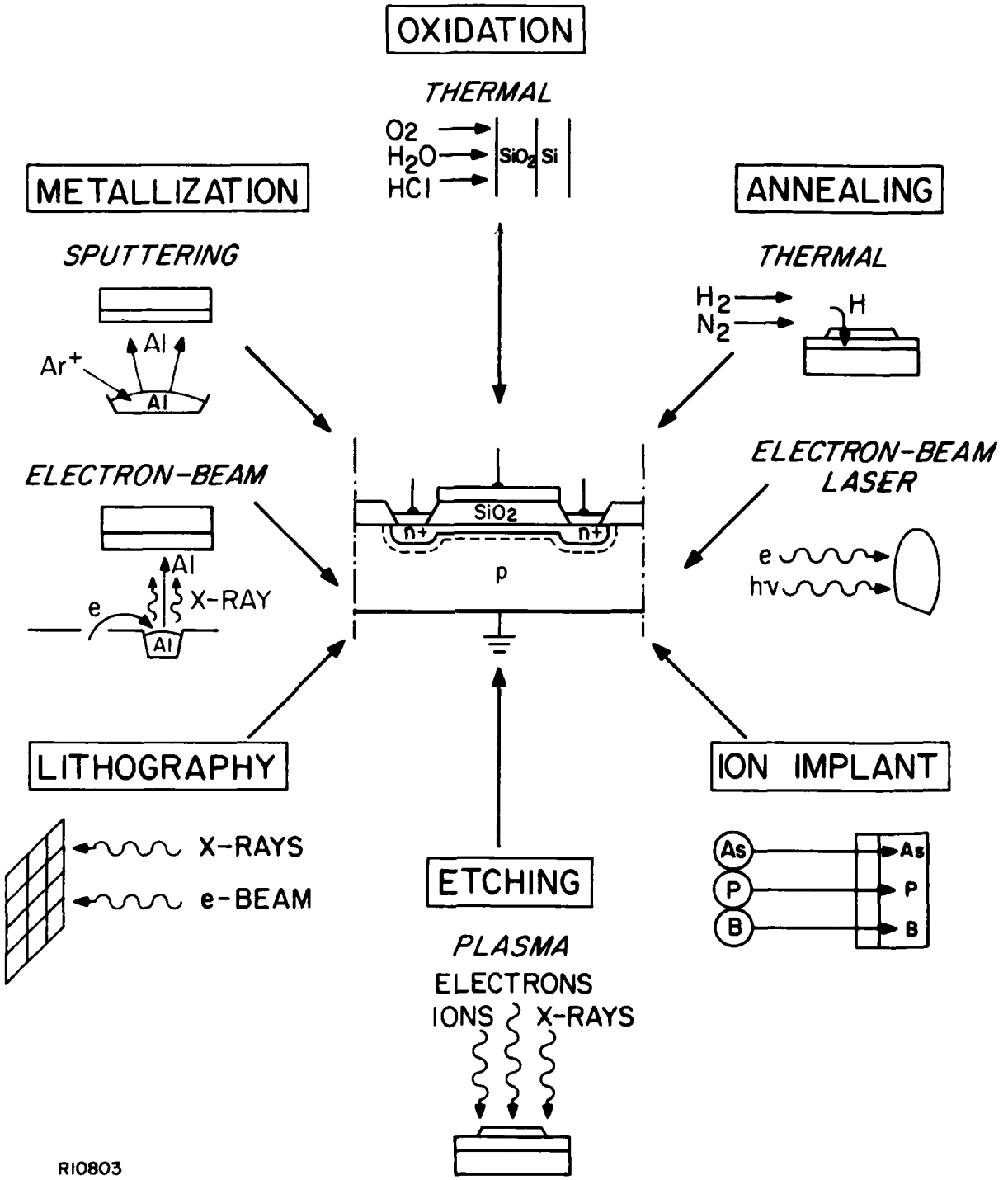

Fig. 2-2. Processes that affect hot carrier trapping in thermal oxides.

channel currents, thermally generated leakage current, and forward bias supply currents can result in carrier injection in the oxide and subsequent trapping. This trapping can affect gain, saturation conductance, and effective threshold voltage (34). These and other adverse effects can cause degradation in both bipolar and MOS devices.

The process dependence of the oxide trapped charge resulting from radiation has been recognized for some time (35) and a similarity between radiation induced hole trapping and avalanche injected hole trapping has been suggested in dry O_2 oxides (36). The process dependence of electron trapping for oxides grown in dry O_2 at 1000°C with different cooling procedures was investigated at 295° and 77°K (37). In this work we examine the process dependence of both electron and hole trapping by avalanche injection and the relationship between avalanche injection and radiation induced carrier trapping. The process parameters investigated include oxidation ambient (dry O_2, pyrogenic steam, and O_2/HCl), oxidation pressure (1, 5, and 10 atm), post-oxidation in-situ anneal ambients (N_2, Ar), cooling ambient and rate (O_2, N_2, and Ar - 3 sec, 2 min, and 10 min), post-metallization anneal ambient (N_2, N_2/H_2, and H_2). Also, the generation of interface states during the avalanche injection process is briefly examined and indicates that interface states are induced during carrier injection.

3.0 EXPERIMENTAL PROCEDURE

3.1 Sample Preparation

The silicon used for the experiments was n-type (100) and (111) of resistivity 0.2-0.3 Ω-cm and p-type (100) and (111) of resistivity 0.4-0.7 Ω-cm. The silicon was produced at Fairchild and was in the form of 2-inch (n-type) and 3-inch (p-type) diameter wafers, chem-mechanically polished on one side and etched on the other side. The samples were cleaned in hot sulfuric acid, aqua regia, 10:1 DI water:hydrofluoric acid, and 2-propanol vapor, with appropriate deionized water rinses. The wafers were then loaded into an oxidation furnace in the appropriate ambient, oxidized for a given time, and then pulled from the furnace either in the oxidizing ambient or in nitrogen or argon. Pull rates varied from 1-3 seconds (fast pull "FP") to 2-10 minutes (slow pull "SP").

Dry oxygen was supplied from a liquid source, as were nitrogen, hydrogen, and argon. The pyrogenic steam oxidations were carried out by the direct reaction of H_2 and O_2 in a pyrogenic system. For the HCl/O_2 oxidations, HCl of 99.99% purity was supplied from a gaseous bottle source. Calibrated flowmeters were used to monitor and control gas mixtures in the proper ratios. The oxidation systems were conventional hot wall, resistance-heated furnaces with quartz tubes and high purity mullite liners.

A high pressure oxidation system (2,38) was used to grow the high pressure oxides. The system consists of a horizontal resistance heated quartz oxidation tube enclosed in a stainless steel shell. Details of the oxidation cycles and pressurization procedure have been described elsewhere (38). The oxide thickness requirement of about 800 Å resulted in a limit on

a maximum pressure of 5 atm during oxidations in pyrogenic steam and 10 atm during oxidation in dry O_2. Oxide thickness was measured by a Gaertner model L116 ellipsometer.

Following oxidation, 1 μm thick Al-Cu-Si* films were vacuum deposited on the oxides by cold flash (no substrate heating) in order to avoid radiation effects from e-beam evaporations. Metal dots approximately 750 μm in diameter were formed by photolithography. Following dot definition the oxide was removed from the back of the wafers and Al-Cu-Si deposited on the back in the manner described above.

One half of each wafer was annealed at 400°C in either nitrogen, hydrogen/nitrogen mixtures, or in hydrogen in order to determine the effects of pre- and post-metallization annealing in hydrogen-containing ambients. Values of fixed oxide charge density (N_f) and interface state density (N_{it}) for each wafer were determined prior to avalanche charge injection. Wafers from each run were sent to the Naval Research Laboratory for radiation exposure and evaluation.

The detailed processing sequence involved in the fabrication of the samples other than the oxidation, anneal, and metallization steps will be discussed in the appropriate section.

3.2 Charge Injection and Measurements

Charge injection was carried out by driving the MOS capacitor structures into deep depletion by means of a large ac signal. The frequency of the applied signal should be

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*Al-4% Cu-2% Si.

sufficient to prevent the formation of an inversion layer while the amplitude is chosen such that the field in the substrate will result in avalanche carrier multiplication. The carriers generated by the avalanche process are then accelerated by the field, with the minority carriers moving towards the Si/SiO_2 interface. Some carriers arriving at the interface will have sufficient energy to surmount the field lowered potential barrier at the interface. Most of the injected carriers drift through the SiO_2 and are collected at the fieldplate. However, a percentage of these carriers are trapped in the oxide and the details of that process are of great interest, as pointed out previously.

Figure 3-1 shows a schematic of the automated trapping system used. The method of injection is similar to that used successfully at IBM (36,39). The measurement is carried out by switching the samples between two circuits, a capacitance measuring circuit and an avalanche injection circuit. The MOS structure is first switched to the C-V circuit and a 1 MHz curve obtained on the virgin capacitor. The capacitor is then switched automatically by the calculator/controller to the injection circuit where an ac signal of predetermined amplitude and frequency is applied. The current flow is monitored by a Keithley 616 electrometer and the value of current kept constant by adjusting the amplitude of the ac signal every 1/3 second. All operations and data gathering are carried out by the calculator/controller through an HP-IB bus. Flat band voltage changes resulting from the avalanche injection are obtained by switching back to the C-V circuit every 70 seconds.

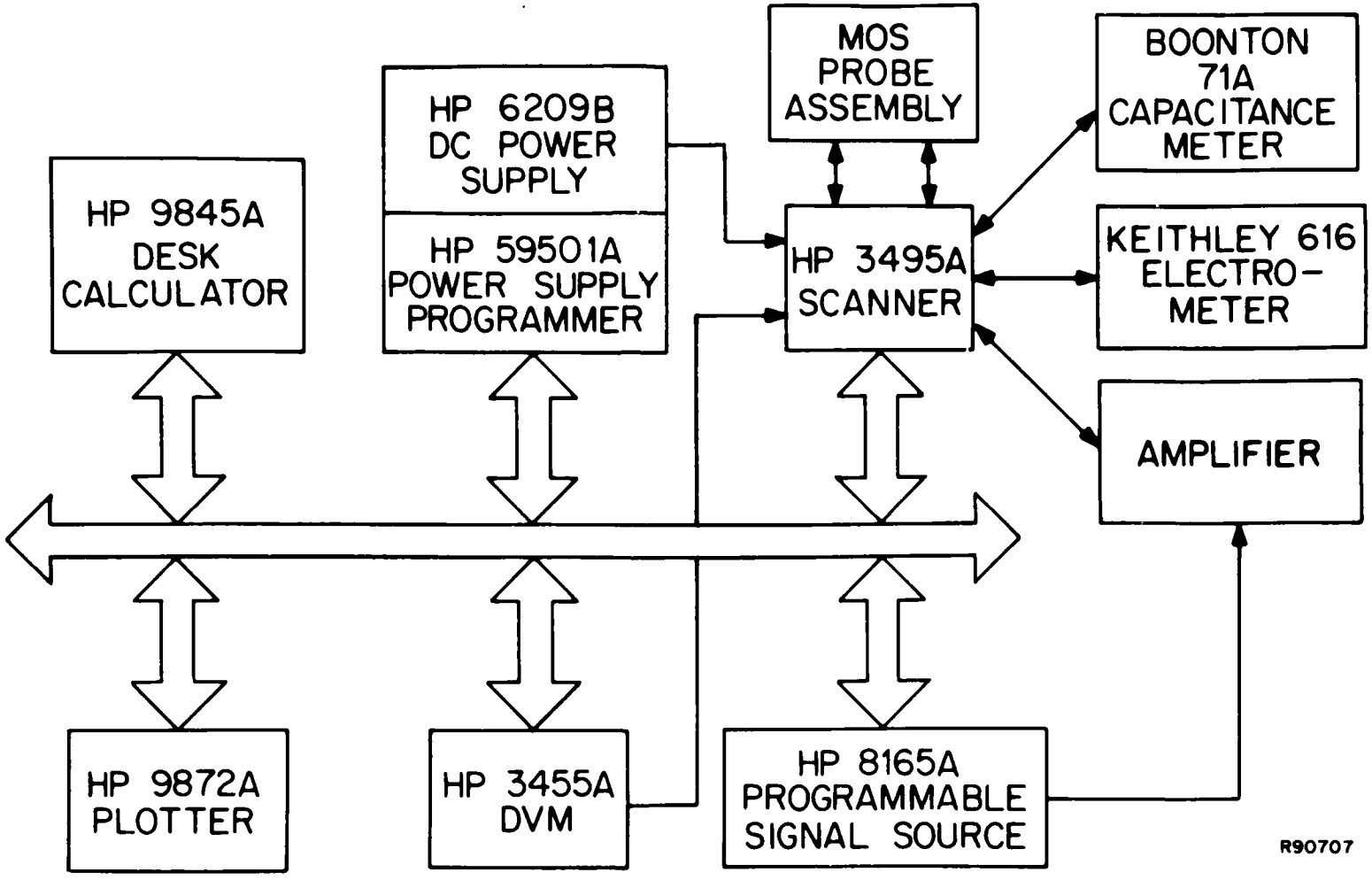


Fig. 3-1. Schematic diagram of the automated avalanche injection and trapping system.

3.3 Data Acquisition and Reduction

Prior to avalanche testing, each wafer is evaluated in terms of fixed oxide charge density (N_f) and interface state density (N_{it}). This information is needed to verify that proper processing techniques have been employed and in order to evaluate any possible relationship between N_f and N_{it} and the density of trapped charge resulting from avalanche injection or radiation exposure.

The effect of process parameters on the density of fixed oxide charges and interface trapped charge has been documented in previous work (11) and the results were used as a further check on the validity and reproducibility of the measurements and the fabrication procedures. Some general guidelines on charge density variations due to process and material parameters are:

(a) Slow pull in oxygen results in the highest level of fixed oxide charge.

(b) Nitrogen or argon slow pulls yield the lowest levels of charges at these temperatures (longer N_2 or Ar anneal times at 900° and 1000°C will reduce fixed oxide charge density further).

(c) The oxygen triangle effect or "N_f-O_2" triangle (8,12,40) can be observed from the oxygen fast pull data.

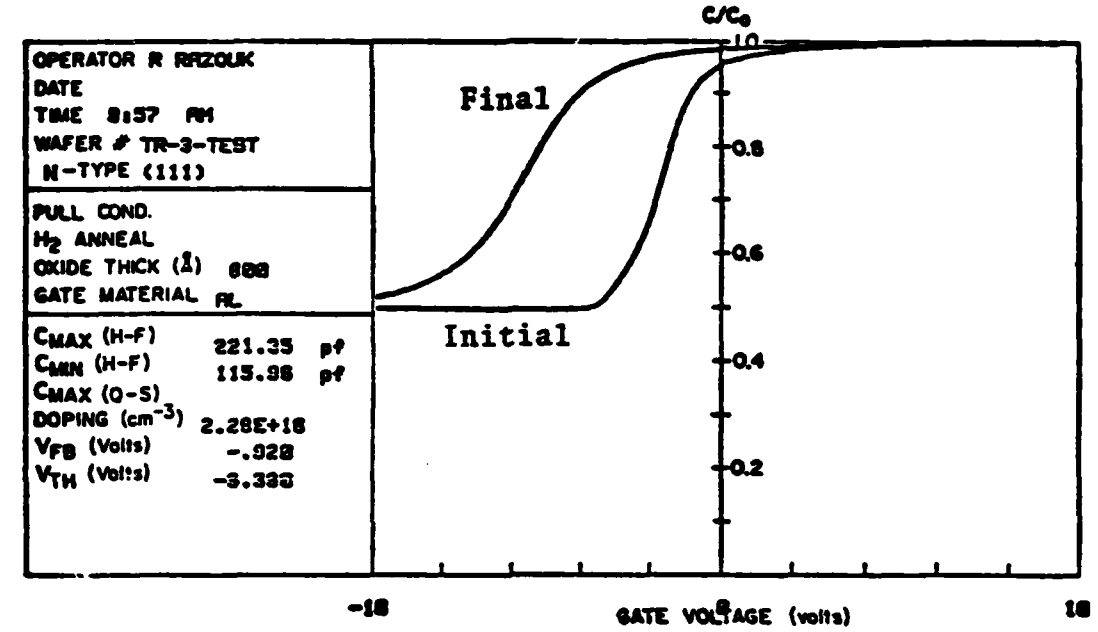
(d) Both N_f and N_{it} are dependent on the orientation of the silicon substrate. The charge densities measured on MOS structures fabrication on (111) silicon substrates are always greater than those fabricated on (100) substrates.

Once the basic data about oxide charges (N_f and N_{it}) have been gathered for each wafer, the avalanche trapping experiments are carried out. A typical output from the system (Fig. 3-2) shows the initial C-V trace at 1 MHz, the final C-V trace following more than 4000 sec of injection time and the flat band voltage shift as a function of time.

Comparison between processes is carried out by recording the flat band voltage shift following 2000 sec of injection time at the appropriate current density. This yields the flat band voltage shift resulting from a given charge flux. Since the flat band voltage shift is directly related to the trapped charge density, the measurement is representative of the amount of charge trapped for a given charge flux.

It should be noted that although flat band voltage shifts (ΔV_{FB}) are used exclusively in the data reported here, interface state density increases can result in threshold voltage changes (ΔV_{TH}) that exceed the change in the flat band voltage. In some cases a decrease in V_{FB} is accompanied by an increase in V_{TH} as it would be in the case of simultaneous electron trapping and generation of donor-like interface states.

Other information available from the measurement consists of capture cross sections and effective trap densities. For first-order rate processes, the trapping-detrapping of thermal carriers can be expressed as:



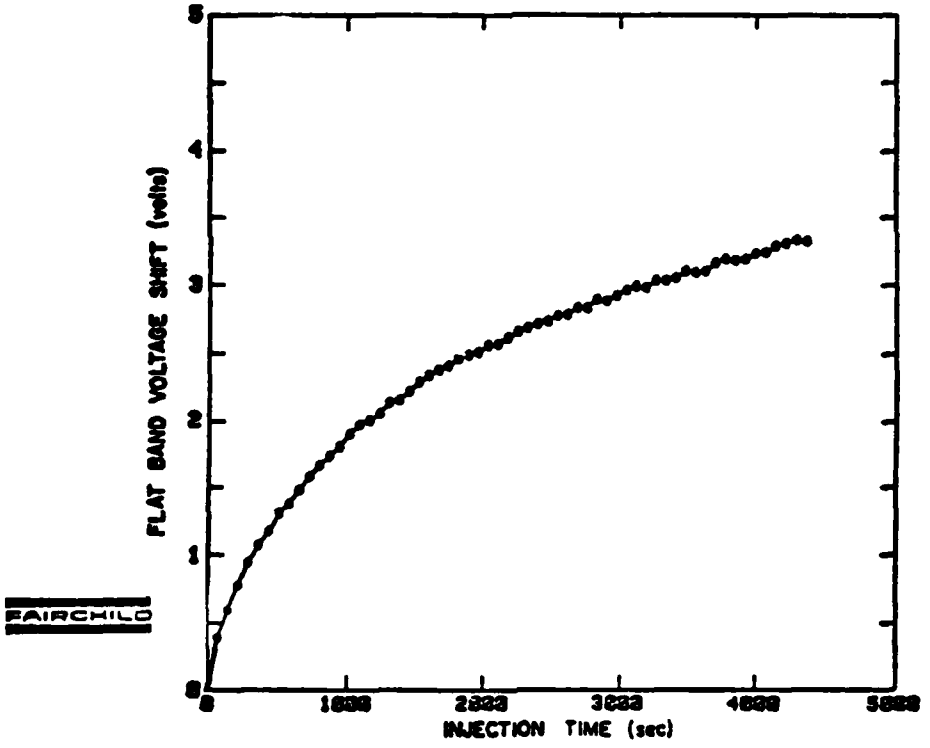


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Fig. 3-2. Typical output from the automated avalanche carrier injection and trapping system.

$$\frac{dn_t}{dt} = \text{capture rate - detrapping by photons - detrapping by phonons}$$

$$\frac{dn_t}{dt} = n_c V_{th} \sigma_c (N - n_t) - F_p \sigma_p n_t - N_c n_t V_{th} \sigma_c e^{-E_t/kT} \qquad [1]$$

where

n_t = trapped charge density
N = total trap density
σ_c = capture cross section
n_c = conduction band electron density
V_{th} = thermal velocity
F_p = photon flux
σ_p = photoionization cross section
N_c = effective density of states in the conduction band
E_t = trap energy depth from the conduction band edge.

For cases where no detrapping is occurring, the trapping probability is proportional to the number of unfilled traps and the shift in flat band voltage is given by

$$\Delta V_{FB} = \frac{qN_{eff}}{C_{ox}} \left(1 - e^{-\sigma_c Jt/q}\right) \qquad [2]$$

where

ΔV_{FB} = flat band voltage shift
C_{ox} = oxide capacitance per unit area
J = current density
t = injection time
q = electronic charge
N_{eff} = effective charge density

by taking the derivative of [2] with respect to time

$$\frac{d}{dt}\ (\Delta V_{FB}) = \frac{d}{dt}\ (V_{FB}) = \frac{qN_{eff}}{C_{ox}} \left(\frac{\sigma_c J}{q}\right) e^{-\sigma_c Jt/q} \qquad [3]$$

and

$$\ln \left[\frac{d}{dt}\ (\Delta V_{FB})\right] = \ln \frac{qN_{eff}}{C_{ox}} \left(\frac{\sigma_c J}{q}\right) - \left(\frac{\sigma_c J}{q}\right) t \qquad [4]$$

A plot of ln [d/dt (V_{FB})] versus injection time will yield a straight line in the case of a single trap. The slope of this line allows the computation of the capture cross section while the intercept gives information about the effective trap density. Although it is possible, if the measurement is carried out for long times (or by increasing the current density), to resolve more than one trapping cross section and trap density, the dominant trapping mechanism has been the primary objective of this investigation. A typical plot of ln [d/dt (V_{FB})] versus time is shown in Fig. 3-3 and indicates a trapping cross section of 3.5×10^{-15} cm^2 and an effective trap density of $2 \times 10^{12}/cm^2$.

The variations in the result from capacitor to capacitor on the same wafer and from wafer to wafer on the same run were minor. Some variations were noted from run to run under identical processing conditions; however, these variations were substantially lower than the 4:1 ratio observed by Aitken and Young (36) between some of their batches. These differences have also been reported by G. W. Hughes (41) who found occasional large variation in radiation hardness from wafer to wafer as well as from run to run under identical processing conditions, and by H. L. Hughes (42) who found correlation

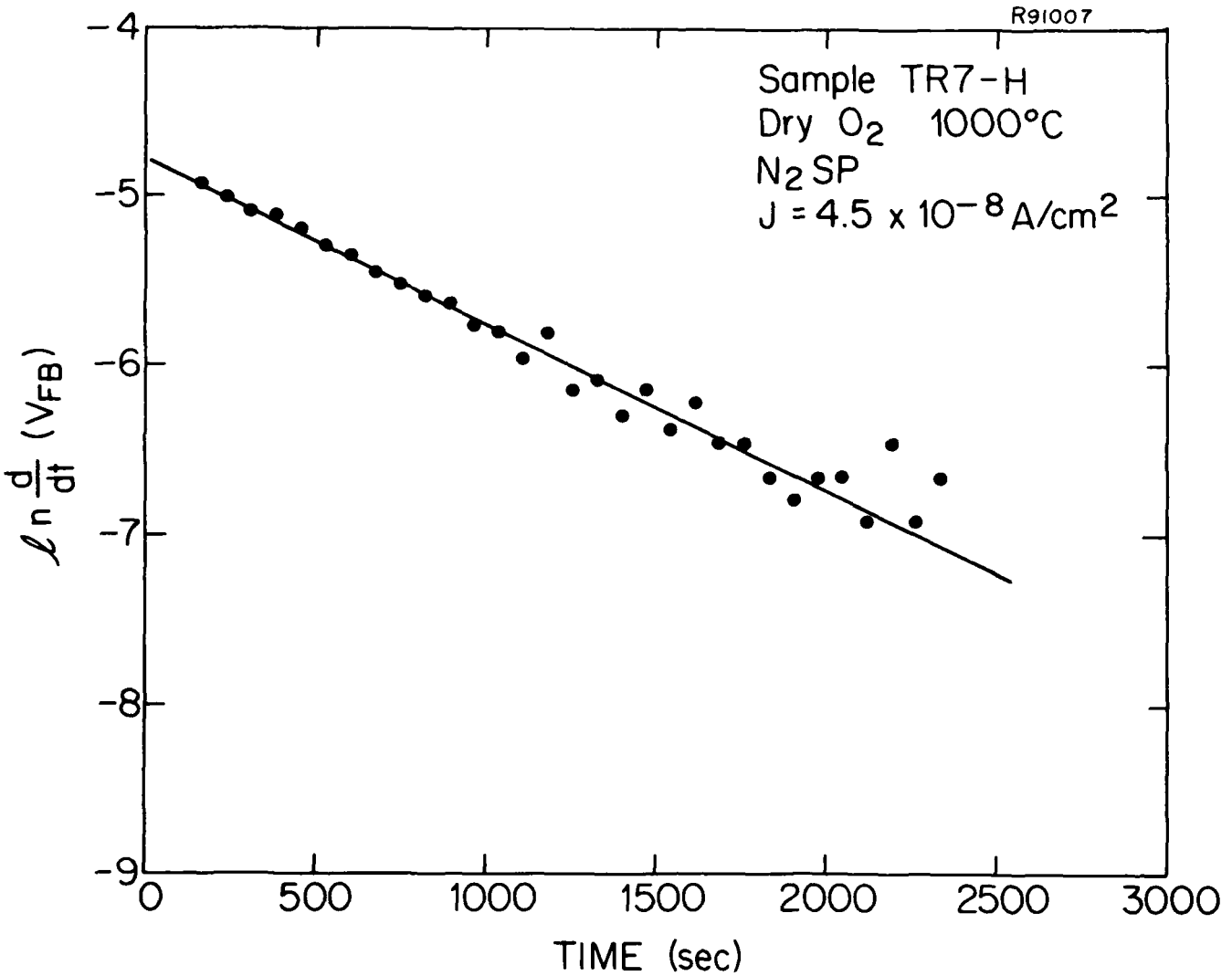

Fig. 3-3. ℓn d/dt (V_{FB}) versus time for samples oxidized in dry O_2 at 1000°C. The sample received an in-situ anneal in nitrogen for 10 min and was cooled in N_2. The post-metallization anneal treatment was: 400°C, 10% H_2 in N_2, 10 min. Current density $J = 4.5 \times 10^{-8}$ A/cm^2.

between silicon surface defects as revealed by Sirtl etch and radiation hardness in MOS structures.

Interface state generation was observed for most samples tested and resulted in a stretch-out of the C-V curves as shown in Fig. 3-4. Quasistatic C-V measurements indicated interface state density increases up to $10^{12}/cm^2$-eV at midgap. The exact nature of the increase in interface states is not known at this time since the trapped charges at the Si/SiO_2 interface could by virtue of their presence or nonuniform distribution result in an "apparent" increase in interface states. The deconvolution of the various contributions could probably be best carried out through annealing treatments known to affect only one of the two charges in question.

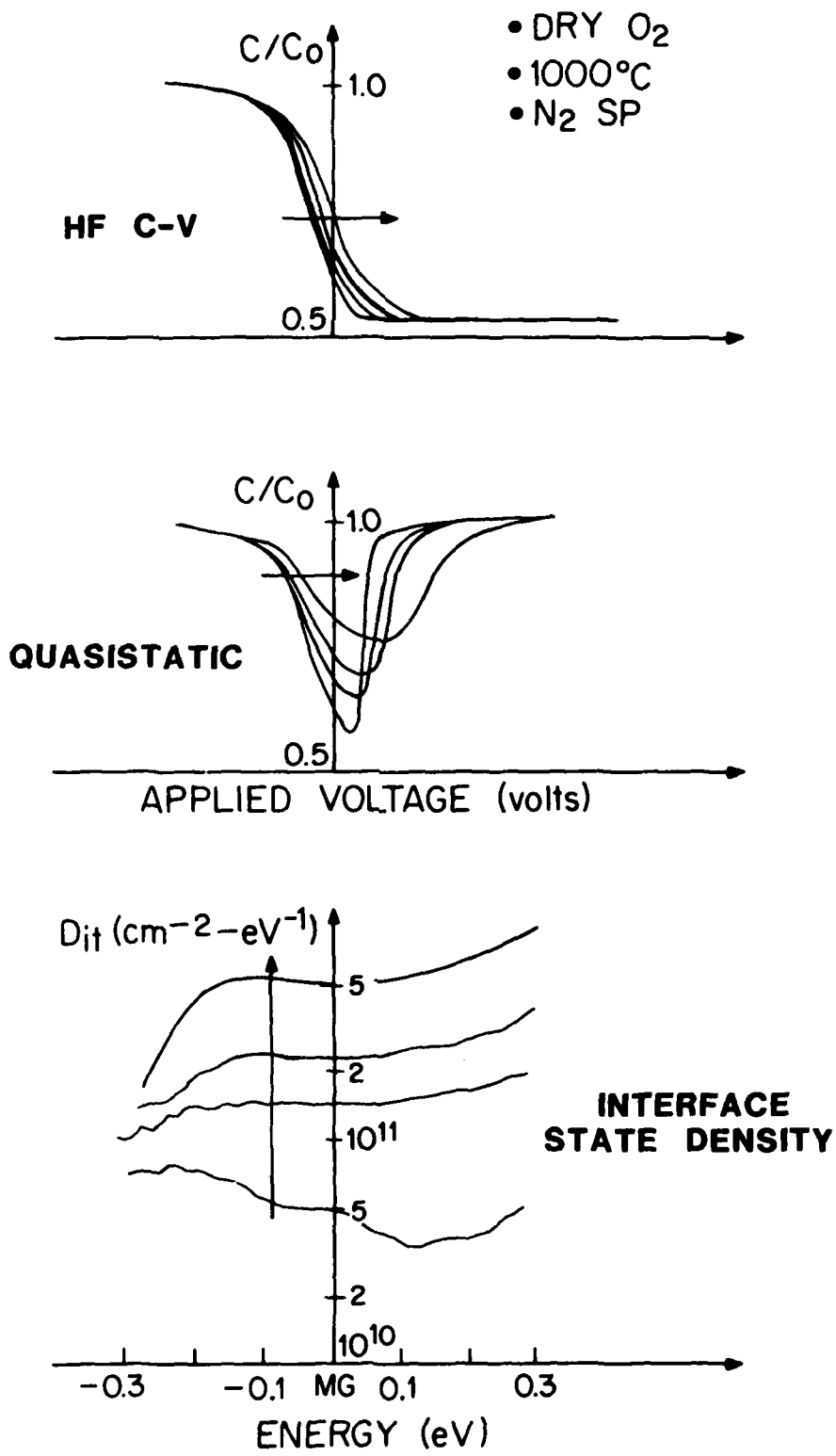

Fig. 3-4. Increase in interface state density as a result of electron injection by avalanche from the substrate.

4.0 RESULTS AND DISCUSSION

4.1 Trapping in Dry O_2 Oxides

N- and p-type (100) and (111) silicon wafers were oxidized in dry O_2 at 800°, 900°, 1000°, and 1100°C. Due to the dependence of the oxidation rate on the orientation of the silicon substrate, the different orientations were oxidized separately in order to achieve the same final oxide thickness (about 800 Å). Following oxidation the wafers were cooled by one of the following conditions:

1 – Wafers cooled in oxygen by rapid pull from the oxidation furnace (oxygen fast pull (O_2FP), 3 sec).

2 – Wafers cooled in oxygen slowly (slow pull in oxygen (O_2SP), 10 min).

3 – Post-oxidation in-situ anneal in nitrogen for 10 min followed by a slow cooling in nitrogen (nitrogen slow pull (N_2SP), 2 min).

3 – Post-oxidation in-situ anneal in argon for 10 min followed by slow cooling in argon (argon slow pull (ArSP), 2 min).

The processing sequences outlined above were chosen because they are representative of typical processing sequences used in the fabrication of MOS integrated circuits. The effect of cooling ambient and rate on the other oxide charges (N_f and N_{it}) is well documented and the potential for a similar dependence of oxide trapped charge (N_{ot}) on process parameters is evident.

4.1.1 Hole Trapping in SiO_2 Grown in Dry O_2

In order to summarize and characterize the data obtained on the effects of process variations on the trapped charge density, the following parameters were always kept constant:

1 – Oxide thickness (800 Å)

2 – MOS capacitor area (4.5×10^{-3} cm^2)

3 – Average current density (4.5×10^{-8} A/cm^2)

4 – Signal frequency (45 kHz)

5 – Prior to measurement all wafers received a 10% H_2 in N_2 post-metallization anneal at 400°C for 20 min.

The effect of the anneal ambient and cooling rate is illustrated in Fig. 4-1. Although all samples are oxidized at the same temperature in dry O_2, the anneal/cool procedure is shown to affect the density of charge trapped following avalanche injection. The least trapping is observed for samples that received no post-oxidation in-situ anneal and that were cooled in the oxidizing ambient (O_2 FP). Nitrogen and argon anneals resulted in flat band voltage shifts at least twice as large as unannealed samples. To summarize and condense the data further, the flat band voltage shift for 2000 sec of injection time will be used to characterize the trapped charge density for a given injected hole flux. The results are illustrated in Fig. 4-2 and indicate that the nitrogen or argon anneal has a notable detrimental effect at 1000°C and above. Cooling in the oxidizing ambient does not result in a clear temperature dependence although oxidations below 1000°C appear to be advantageous.

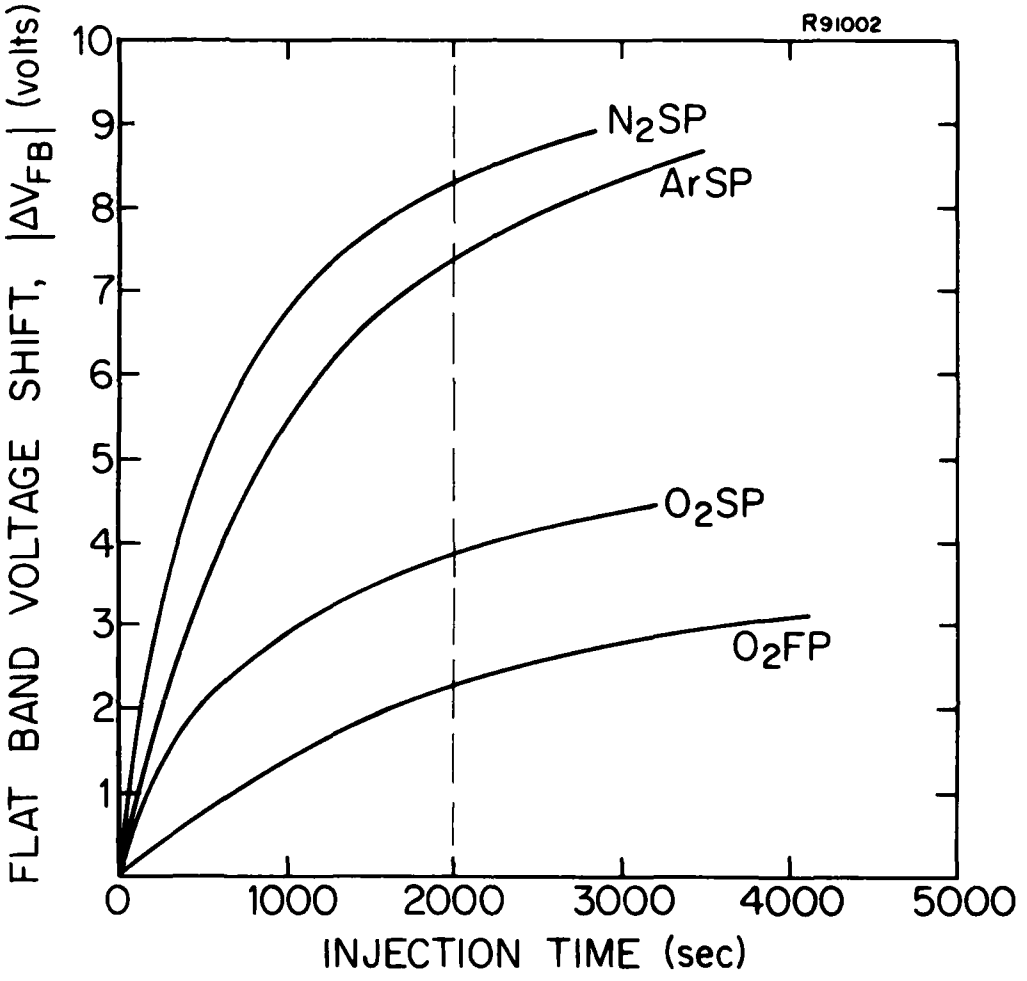

Fig. 4-1. Flat band voltage shift versus injection time for hole trapping from n-type (111) silicon oxidized in dry O_2 at 1000°C. Current density J = 4.5×10^{-8} A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.

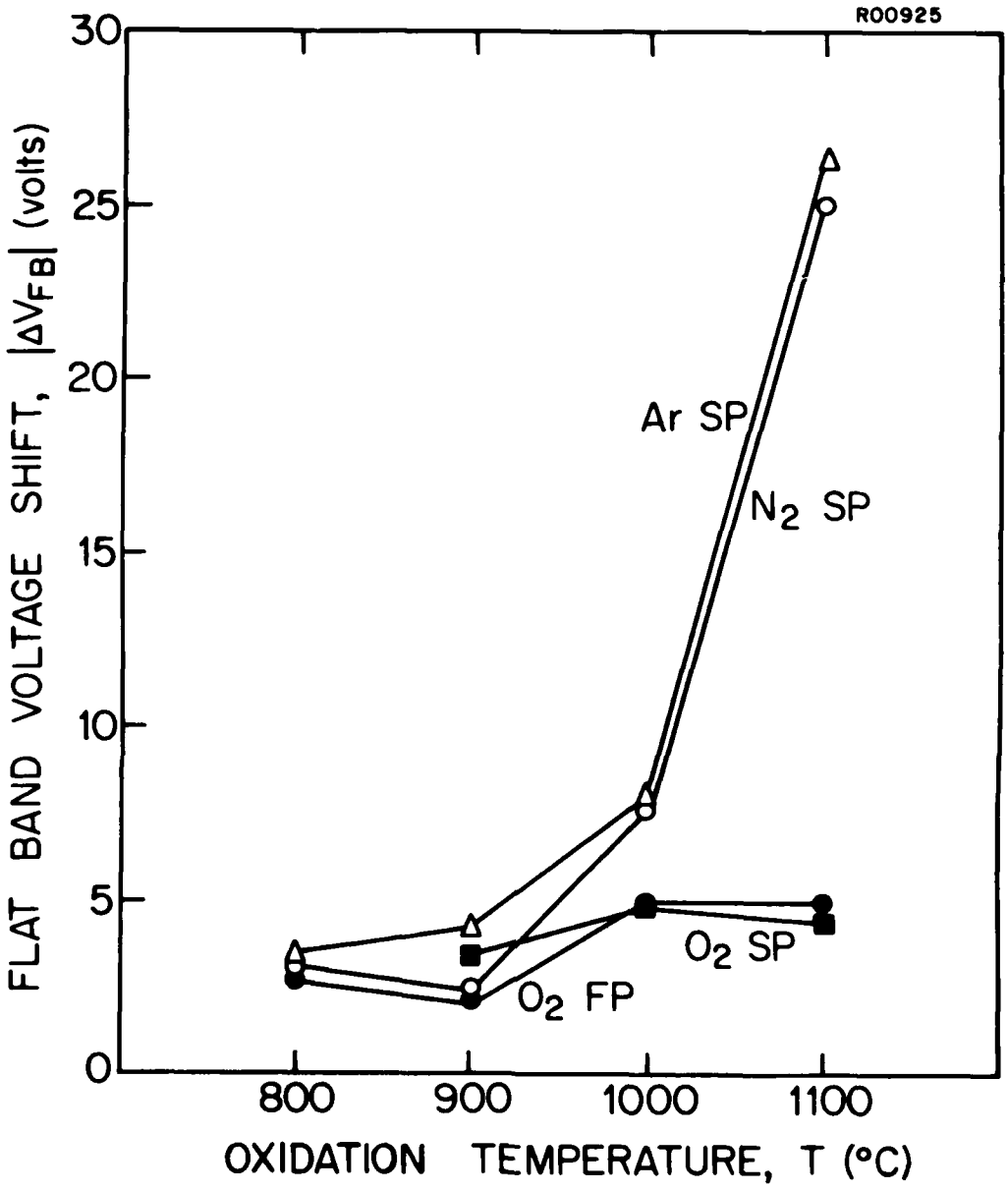

Fig. 4-2. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in dry O_2. Flat band voltage shifts are for 2000 sec injection time. Current density 4.5×10^{-8} A/cm^2.

The effects of substrate orientation on the trapping results are summarized in Fig. 4-3. Flat band voltage shifts for (111) oriented substrates are shown as dashed lines. It should be noted that, in the case where the injected carriers are trapped in the bulk of the oxide layer, an orientation dependence is not expected. The data of Fig. 4-3 however show a clear orientation dependence, particularly in the case of nitrogen or argon annealed and cooled samples. This orientation dependence suggests that:

1 – A possible link exists between the oxide trapped charge N_{ot} and either N_f or N_{it} or both since these two charge densities have clear orientation dependences.

2 – The injection of carriers across the Si/SiO_2 interface during the avalanche injection measurement results in the generation of interface states. This interface state generation has a rate that is dependent on the nature of the interface and therefore its orientation.

3 – The flat band voltage shift cannot be related to a purely surface effect since in that case one would expect a ratio of flat band voltage for (111) to (100) orientation of about three as is the case with fixed oxide charge and interface trapped charge densities N_f and N_{it}. This is clearly not the case, as observed in Fig. 4-3, indicating a combination of bulk and interface traps.

It should be noted that the flat band voltage shifts measured contain contributions from both the trapped charge and any generated interface states. In either case, for hole trapping, minimum charge trapping is obtained when a (100)

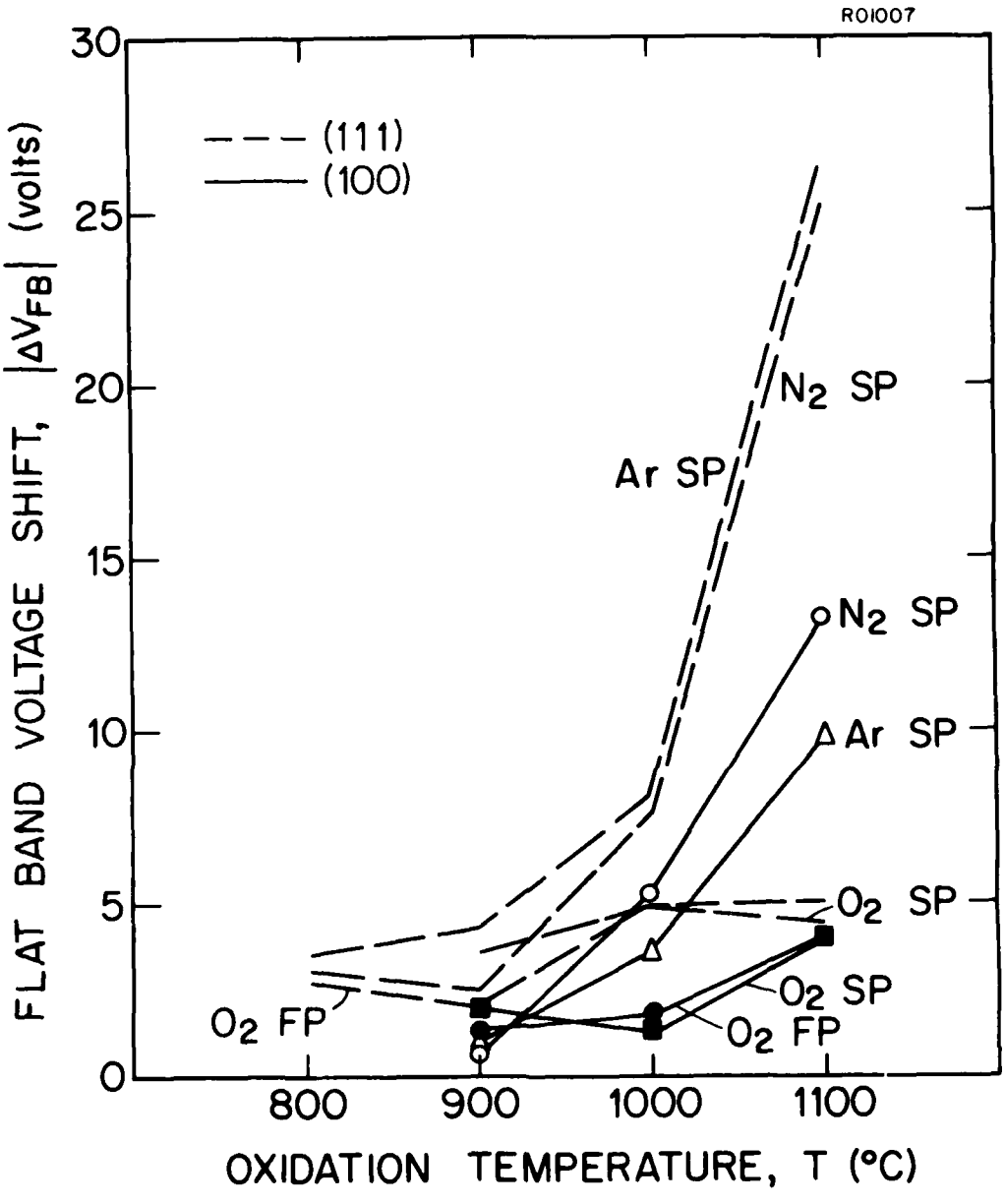

Fig. 4-3. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (100) and (111) substrates. Same conditions as for Fig. 4-2.

oriented substrate is used. Comparison with the charge trapped as a result of radiation exposure is included in a later section.

4.1.2 Electron Trapping in SiO_2 Grown in Dry O_2

Electron injection was carried out from p-type (100) and (111) oriented substrates of 0.4-0.7 Ω-cm resistivity. The same process conditions investigated for the hole trapping experiments are used here with the oxide thickness, capacitor area, and signal frequency held constant. The average current density however was increased to 1.5×10^{-5} A/cm^2 due to the lower trapping efficiency for electrons. The process dependence of electron trapping for (111) oriented substrates is shown in Fig. 4-4 and indicates the following:

(a) The electron trapping efficiency as evidenced by the average current and change in flat band voltage is much lower than the hole trapping efficiency as reported in the literature.

(b) The least amount of trapping occurs at higher oxidation temperatures (1100°C).

(c) Variations in post-oxidation anneal ambients and cooling rates have a minor effect on the amount of flat band voltage shift observed.

Comparison between (100) and (111) oriented substrates however yielded some ambiguous results and possible inconsistencies. The results are outlined in Fig. 4-5. With the exception of the N_2 SP results, an increase in flat band voltage shift is observed with increasing temperature. This effect is quite striking for the oxygen fast pull data. The increased electron trapping observed is quite unexpected and

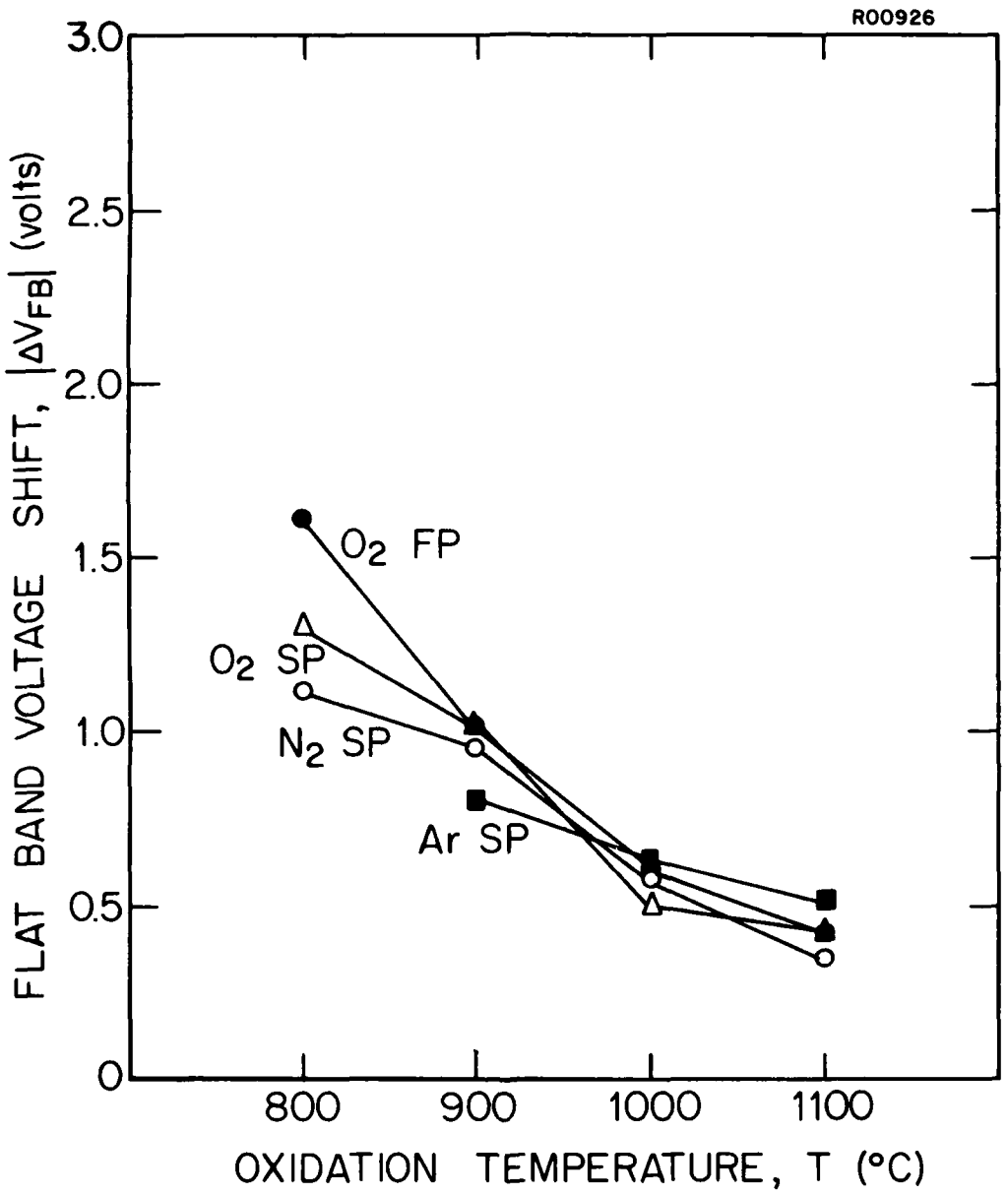

Fig. 4-4. Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (111) substrates. Samples were oxidized in dry O_2 and received a post-metallization anneal at 400°C in a 10% H_2 in N_2 ambient for 10 min. Flat band voltage shifts are for 2000 sec injection time. Current density $J = 1.5 \times 10^{-5}$ A/cm^2.

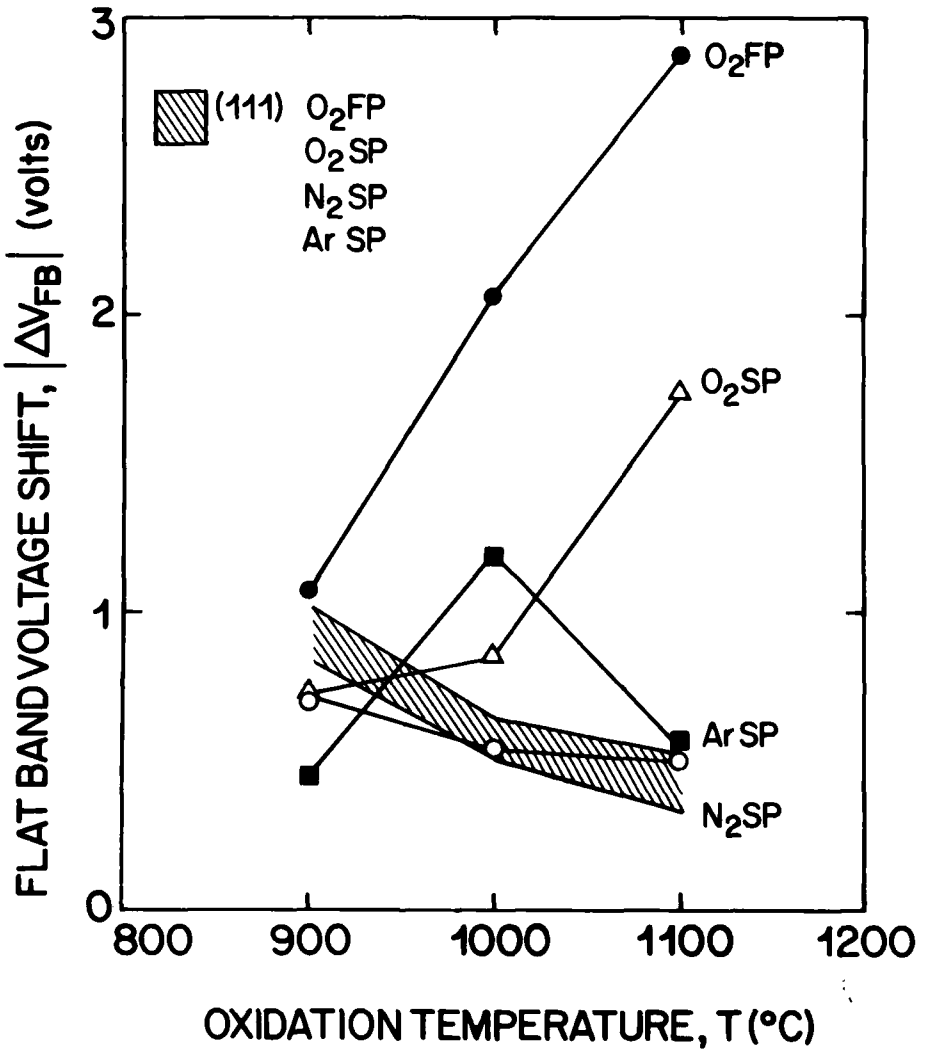

Fig. 4-5. Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (100) and (111) substrates. Same conditions as Fig. 4-4.

cannot be accounted for at this time. A possible explanation however might be the extreme sensitivity of electron trapping to moisture content. Since the (100) and (111) oriented substrates were not oxidized at the same time, a change in the residual moisture content of the oxygen may account for the increased trapping. The post-oxidation anneal in nitrogen or argon would reduce the effect as will be discussed in the section on steam oxidation. These results suggest that accurate monitoring of ambient residual moisture below 1 ppm may be required to completely eliminate or reduce electron trapping in oxides grown in dry O_2. A more detailed study of this effect is warranted.

4.2 Trapping in Pyrogenic Steam Oxides

N- and p-type (100) and (111) silicon wafers were oxidized in pyrogenic steam at 900°, 1000°, and 1100°C. Substrates with differing orientations were oxidized separately in order to achieve the same final oxide thickness. Following oxidation the wafers were cooled by one of the following conditions:

1 – Wafers were cooled in the steam ambient by rapid pull from the furnace (H_2OP, <30 sec).

2 – Post-oxidation in-situ anneal in nitrogen for 10 min followed by a slow cooling in nitrogen (nitrogen, slow pull (N_2SP), 2 min).

3 – Post-oxidation in-situ anneal in argon for 10 min followed by a slow cooling in argon (ArSP, 2 min).

These processing sequences were chosen in order to investigate the effect of steam oxidation on the oxide trapped charge as well as the possibility of removing the oxide traps by annealing in a neutral ambient such as nitrogen or argon.

4.2.1 Hole Trapping in Steam Grown Oxides

Hole injection was carried out from n-type (100) and (111) oriented silicon substrates of 0.2-0.3 Ω-cm resistivity. The average current density used was 4.5×10^{-8} A/cm^2, the same current density used for the dry O_2 experiments. The results for (111) oriented substrates are summarized in Fig. 4-6 and indicate the following:

(a) Oxidations in a steam ambient with a steam cool result in an increase in the flat band voltage shift by a factor of 2 or more when compared to oxidation/cool processing in dry O_2.

(b) Post-oxidation in-situ anneals in nitrogen or argon result in substantial reductions in hole trapping, as evidenced by the smaller flat band voltage shifts, but only for oxidations at 900° and 1000°C. At 800°C, results show a substantial increase particularly for nitrogen annealed samples.

(c) Comparison between (100) and (111) oriented substrates is shown in Fig. 4-7 and indicates that (100) oriented substrates yield smaller trapped charge densities than (111) oriented substrates in agreement with the finding for hole trapping in oxides grown in dry O_2.

(d) Flat band voltage shifts measured for post-oxidation in-situ anneals indicate that the anneal ambient is crucial to the trapped charge density. This is evident from the finding that $|\Delta V_{FB}|$ is approximately the same for both dry O_2 and steam oxides annealed in N_2 or Ar for all oxidation temperatures and for both substrate orientations (Figs. 4-3 and 4-7).

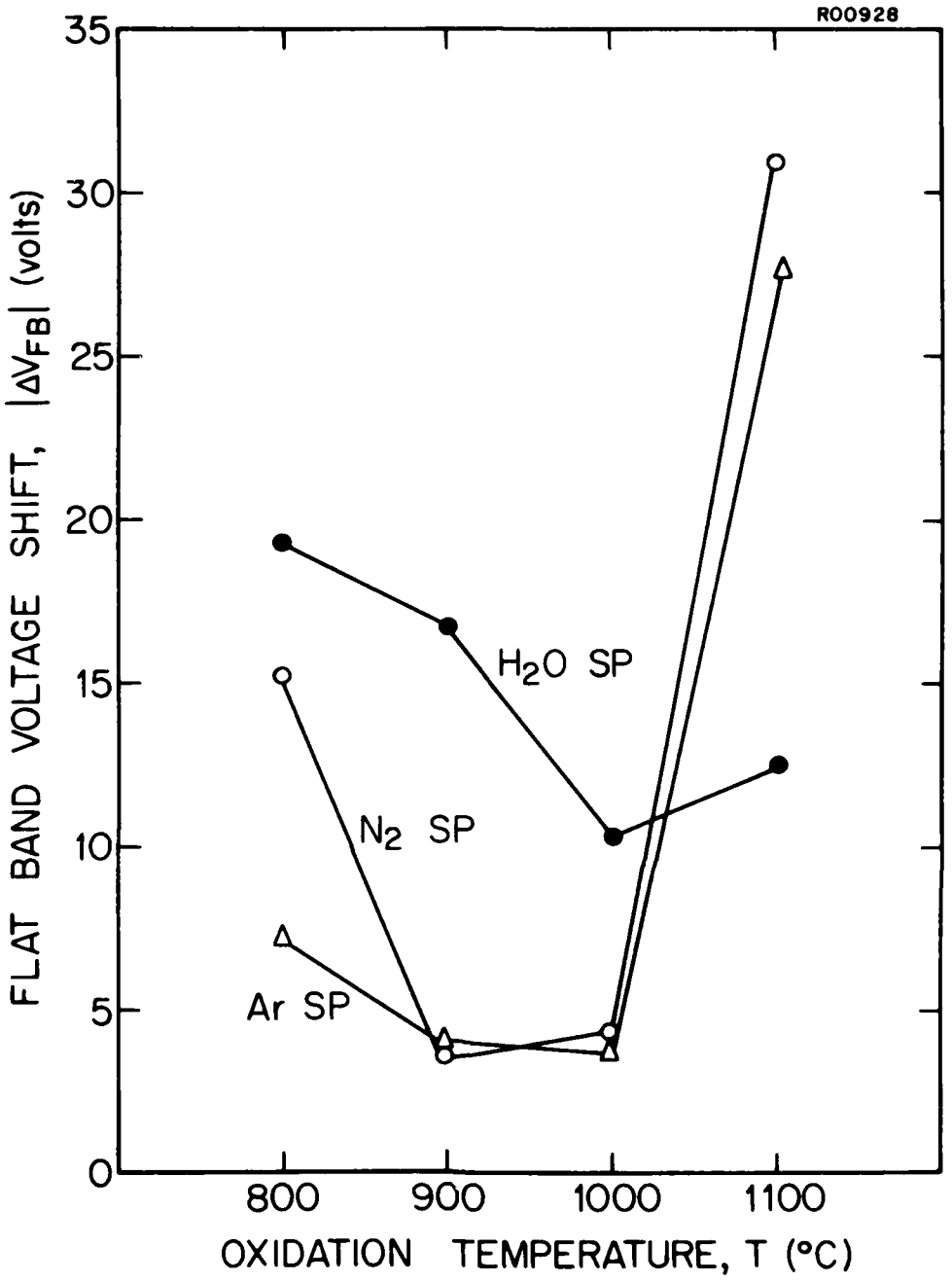

Fig. 4-6. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in steam. Post-metallization anneal at 400°C, 10% H_2 in N_2, 10 min. Flat band voltage shifts are for 2000 sec injection at $J = 4.5 \times 10^{-8}$ A/cm^2.

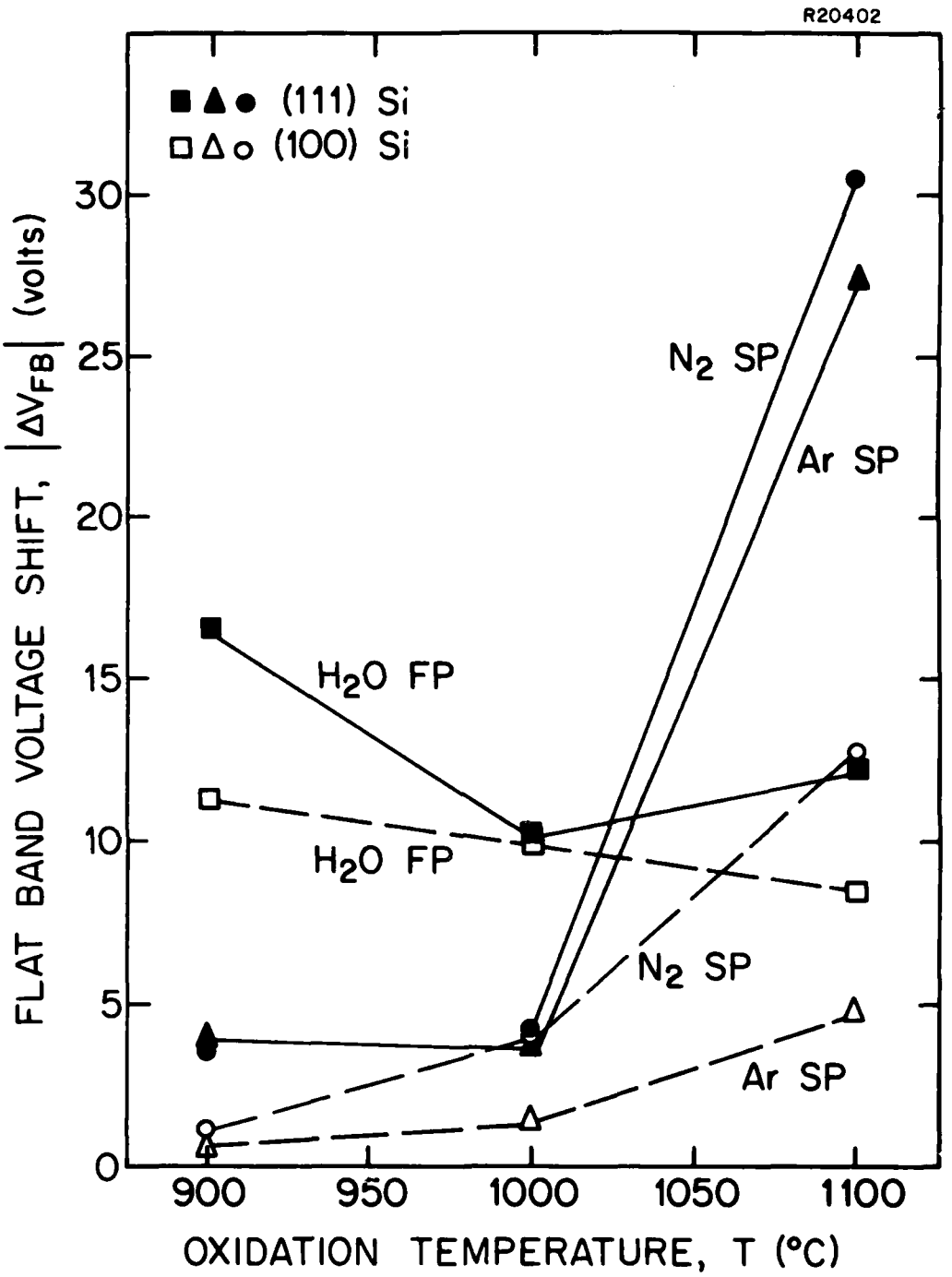

Fig. 4-7. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (100) and (111) substrates. Same conditions as Fig. 4-6.

(e) Comparison between dry O_2 and steam oxidized samples indicates that the difference between nitrogen and argon anneals is real, particularly at the higher temperatures. This is evident from both Fig. 4-3 and Fig. 4-6, which show that argon anneals result in a smaller trapped hole density. This effect may be due to differences in the purity of nitrogen and argon and again highlights the importance of residual contaminations in the gases used.

In summary, the major results in the investigation of hole trapping for dry O_2 and steam oxidations at 1 atm indicate that (100) orientations and low temperature, low moisture processing are necessary for minimum hole trapping in thermal oxide.

4.2.2 Electron Trapping in Steam Grown Oxides

Electron injection was carried out from p-type (100) and (111) oriented silicon substrates 0.4-0.7 Ω-cm in resistivity. The average current density used as well as other process and measurement parameters remain the same as in the dry O_2 investigation. Characteristic of electron trapping in thermal steam grown oxides is the "N" shaped flat band voltage versus injection time curve. Following an initial increase in flat band voltage with injection time, a decrease is observed followed by a subsequent increase. This is shown in Fig. 4-8 for electron trapping from p-type (111) silicon oxidized in pyrogenic steam at 900°C. This effect has been previously reported in the literature (19) and it has been proposed that interface state generation may be associated with this behavior. Figure 4-9 shows just how the generation of the appropriate type of interface state during the avalanche injection process can lead to a reduction in the flat band voltage shift. The H-F C-V curve shift to the right from (1) to (2) indicates electron

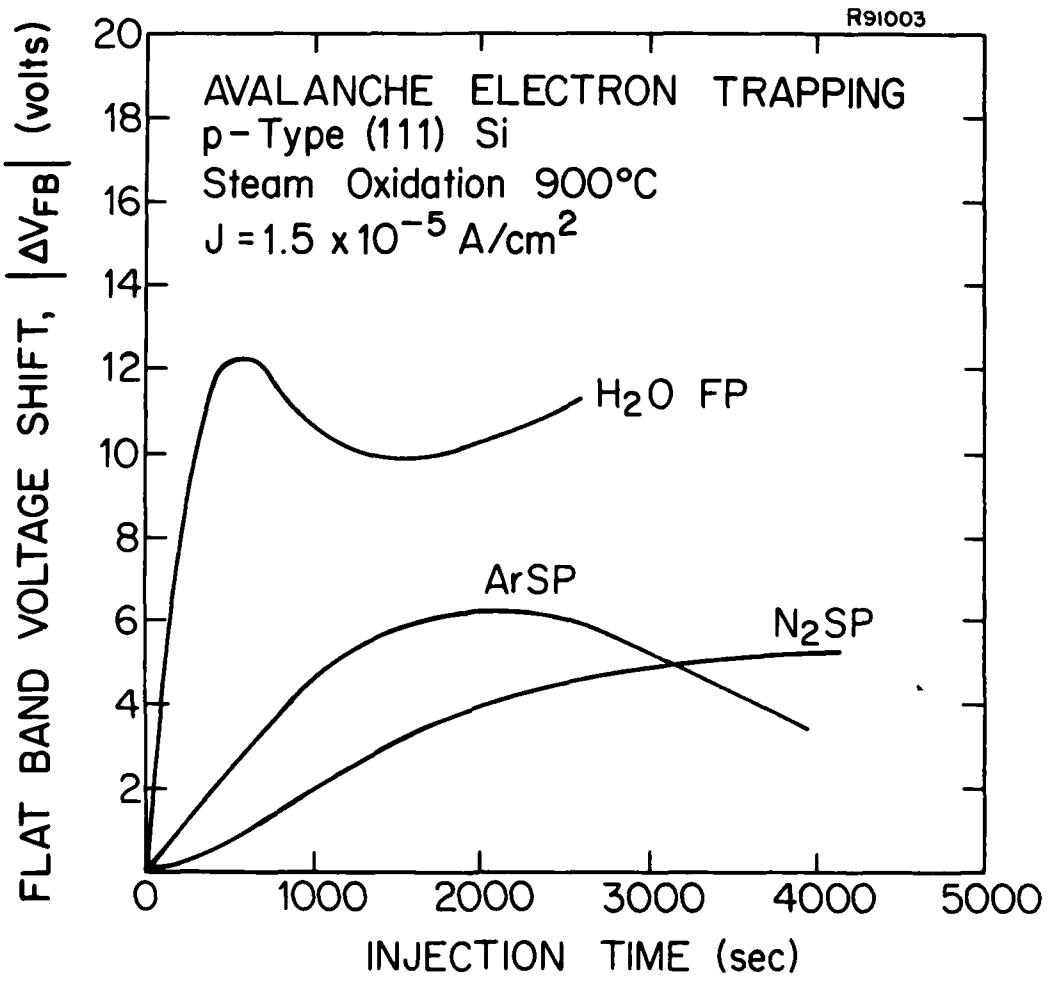

Fig. 4-8. Flat band voltage shift versus injection time for electron trapping from p-type (111) silicon oxidized in steam at 900°C. Current density $J = 1.5 \times 10^{-5}$ A/cm^2 and PMA = 400°C/10% H_2 in N_2/10 min.

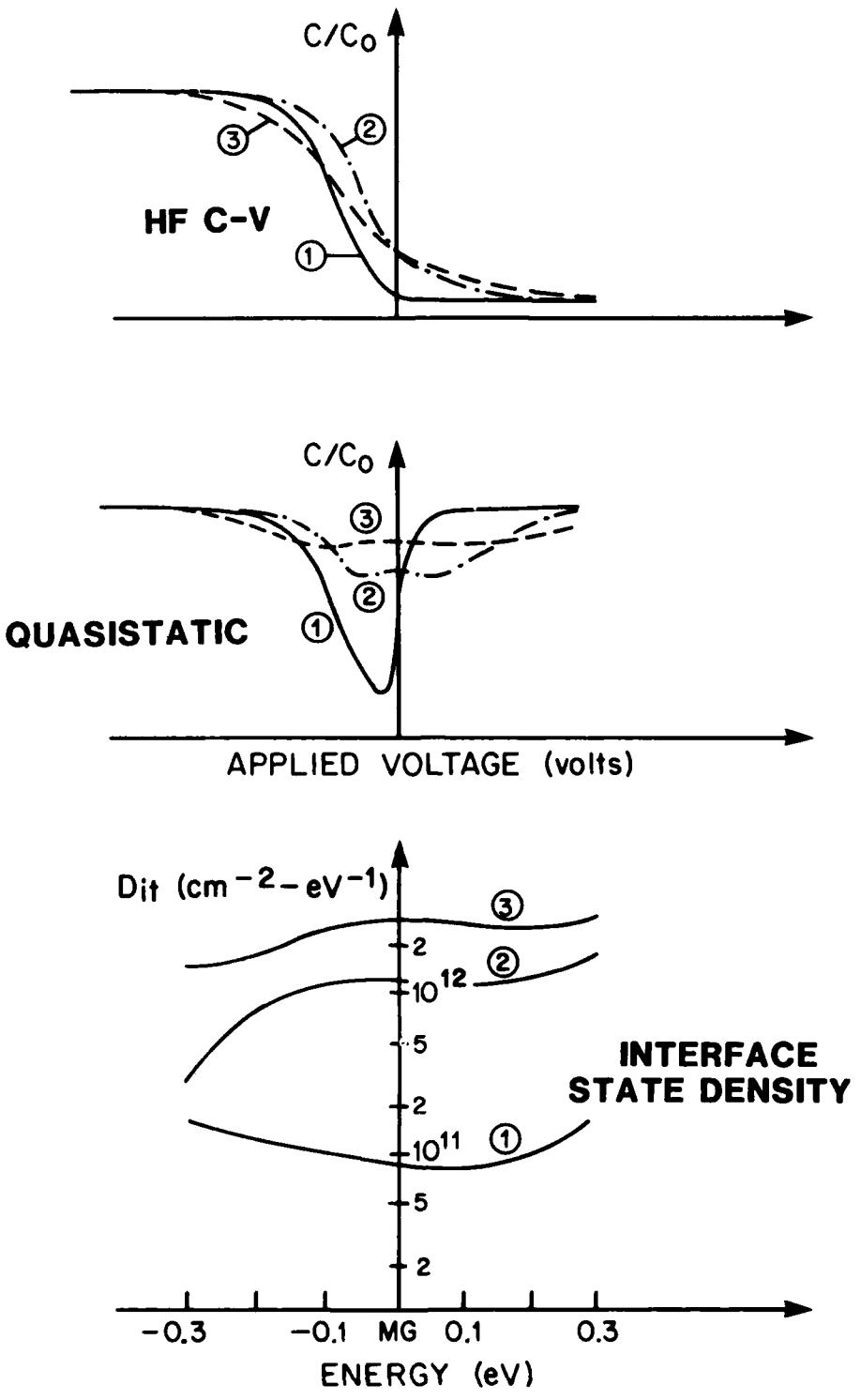

Fig. 4-9. Change in HF C-V curve during avalanche electron injection in steam grown oxides.

trapping, while the quasistatic measurement indicates an increase in interface state density. From (2) to (3), a reduction in flat band voltage shift is seen associated with a further increase in interface state density. The type of interface states generated, donor-like for this case, would result in the flat band voltage shift observed. It should be noted that whereas the flat band voltage shift is reduced, the threshold voltage shift $|\Delta V_{TH}|$ continues to increase.

A summary outlining the process dependence of electron trapping in steam grown oxides is shown in Fig. 4-10 for oxides grown on both (100) and (111) oriented substrates. The results indicate the following trends:

(a) Oxidation in a steam ambient results in a substantial increase in the density of trapped electrons following avalanche charge injection when compared to oxidation in a dry O_2 ambient.

(b) Post-oxidation annealing in nitrogen or argon is very effective in reducing the density of trapped electrons to levels similar to those obtained in dry O_2 oxidations. The annealing however is only effective at 1000°C and above and is least effective at 800°C.

(c) An orientation dependence can be seen for the steam cooled oxides only. For nitrogen and argon annealed oxides the results show no clear pattern of orientation dependence. This is the same result obtained for dry O_2 oxides.

(d) The high levels of trapping following post-oxidation anneal in N_2 or Ar at 800°C are worth noting. Longer anneal times at the lower temperatures may be needed

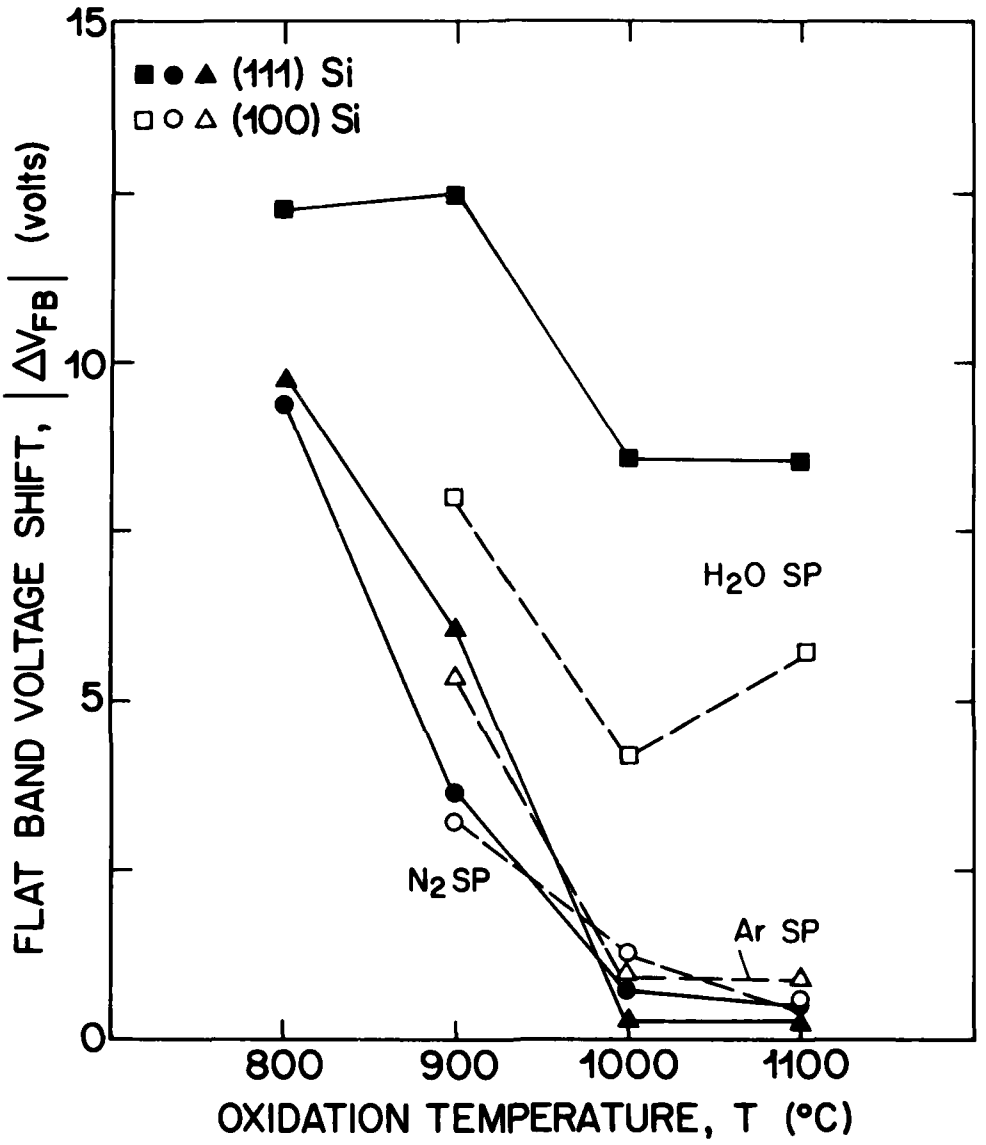

Fig. 4-10. Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (100) and (111) substrates.

to reduce trapping. Also of importance is the decrease in trapping with increasing temperature and with inert gas anneals at all temperatures. This behavior is typical of fixed oxide charge both in dry O_2 and in steam oxides. Some correlation seems to be present between electron trapping and the levels of positive fixed oxide charge, particularly in dry oxides or oxides annealed in N_2 or Ar. Electron trapping could be occurring both on water related sites and possibly on positive fixed charge sites. A more thorough examination of the possible relationship between fixed oxide charge and interface state densities and the oxide trapped charge density for both electrons and holes will be presented in Section 4.8.

4.3 Trapping in O_2/HCl Grown Oxides

N- and p-type (111) silicon wafers were oxidized in a 5% HCl/O_2 ambient at 1000°C. All wafers received a post-oxidation in-situ anneal in argon or nitrogen. The results can be summarized as follows:

(a) Flat band voltage shifts exceeding 16 V (average current density 4.5×10^{-8} A/cm^2, 45 kHz, 2000 sec) were recorded, the highest for hole trapping at 1000°C for both dry O_2 and steam grown oxides. Differences between Ar and N_2 post-oxidation anneals were minor. The increased trapping in the samples is clearly related to the chlorine presence in the oxide, predominantly at the Si/SiO_2 interface since trapping due to water related sites, a by product of the O_2/HCl reaction, was shown to be minimized following a 10 min N_2 or Ar anneal at 1000°C. Even

though the presence of chlorine at the Si/SiO_2 interface does not seem to have a considerable effect on fixed oxide charge and interface states, it could act as traps for holes injected from the substrate.

(b) Electron trapping characteristics differed substantially once more from hole trapping characteristics. Flat band voltage shifts of approximately 1 V were observed. Results were similar to dry O_2 oxides or H_2O oxides annealed in N_2 or Ar.

From the above results, oxidation in an ambient containing HCl can add to the density of trapped holes in the oxide. No clear effect is noted for electron trapping.

4.4 Trapping in Oxides Grown at High Pressure

N- and p-type (100) and (111) oriented silicon wafers were oxidized in dry O_2 and in pyrogenic steam in a high pressure oxidation system. Oxidation temperatures investigated are 800°-1000°C at 10 atm in dry O_2 and 800°C, 5 atm in pyrogenic steam. The oxidation in steam could not be carried out at a higher pressure due to the rapid oxidation rate resulting from the increased pressure coupled with the thin oxide requirement (800 Å).

A typical high pressure oxidation cycle, representing a dry O_2 oxidation, is shown in Fig. 4-11. It should be noted that the pressurization time varied with final oxidation pressure and that all oxidations are terminated with a nitrogen depressurization cycle and a subsequent nitrogen in-situ anneal. Further details on the high pressure oxidation procedures, the oxidation kinetics and the effect of pressure on fixed oxide charge and interface trapped charge densities have been presented elsewhere (38,43).

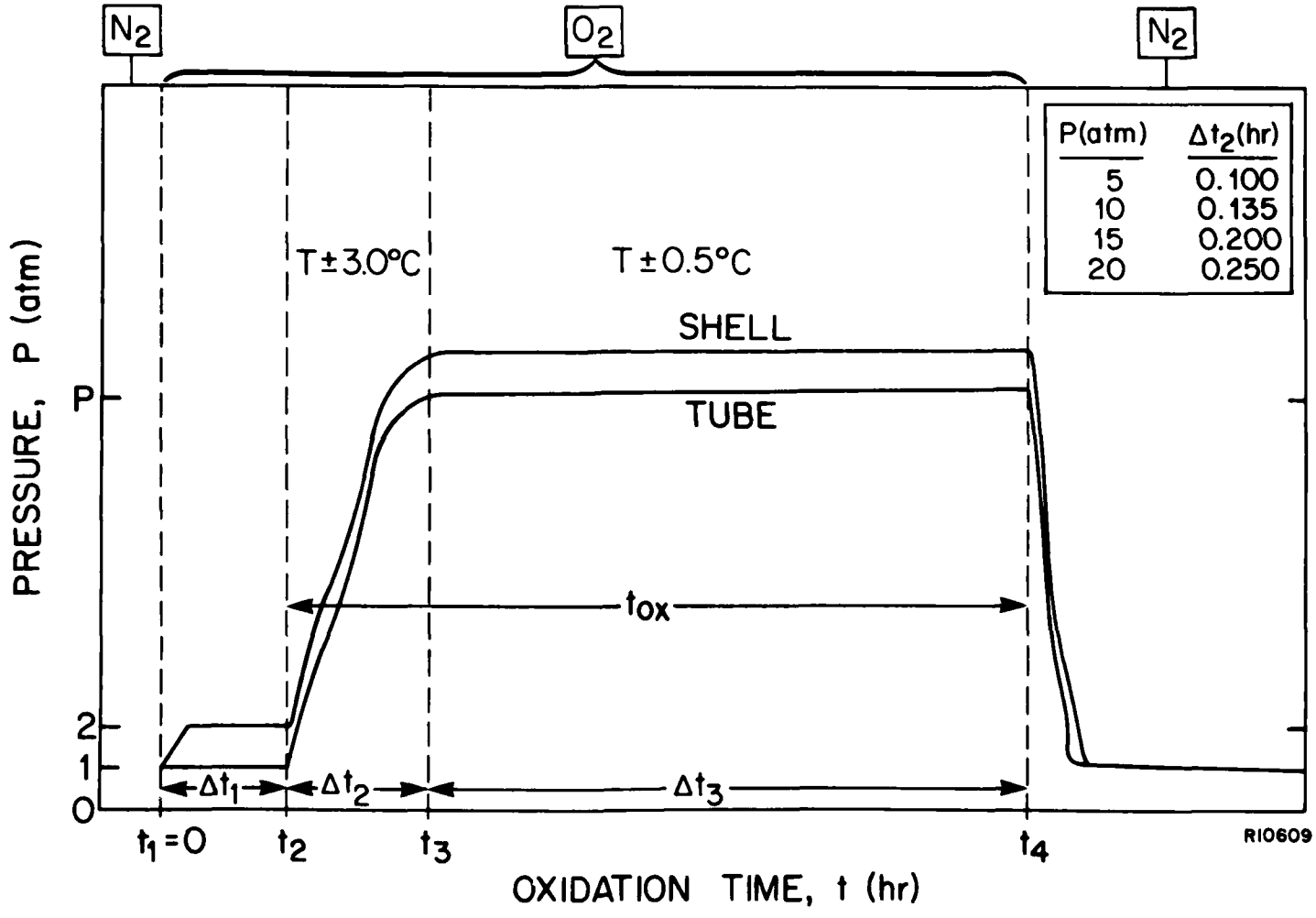

Fig. 4-11. Typical high pressure oxidation cycle in dry O_2 showing process sequence and pressurization time.

4.4.1 Hole and Electron Trapping in Dry O_2 Oxides

Flat band voltage shifts due to hole trapping in oxides grown at 1 and 10 atm at various temperatures are shown in Fig. 4-12. Comparison between the high pressure and 1 atm oxides (annealed in nitrogen in situ following oxidation) indicates that:

(a) The orientation effect observed for hole trapping in oxides grown at 1 atm is present in high pressure grown oxides.

(b) The density of trapped holes is slightly higher in high pressure oxides.

(c) The increase in $|\Delta V_{FB}|$ observed at 800°C (over that at 900°C) is also observed at the higher pressure (10 atm).

Flat band voltage shifts due to electron trapping are shown in Fig. 4-13 for oxides grown at 1 and 10 atm in the range of 800°-1100°C. Results show that no clear orientation dependence exists and there is an increase by a factor of almost 5 in the density of trapped electrons for a higher pressure oxidation cycle. This increase may be a direct result of the difficulty in controlling residual moisture in a high pressure oxidation system as well as the previously mentioned sensitivity of electrons trapping due to ambient moisture content.

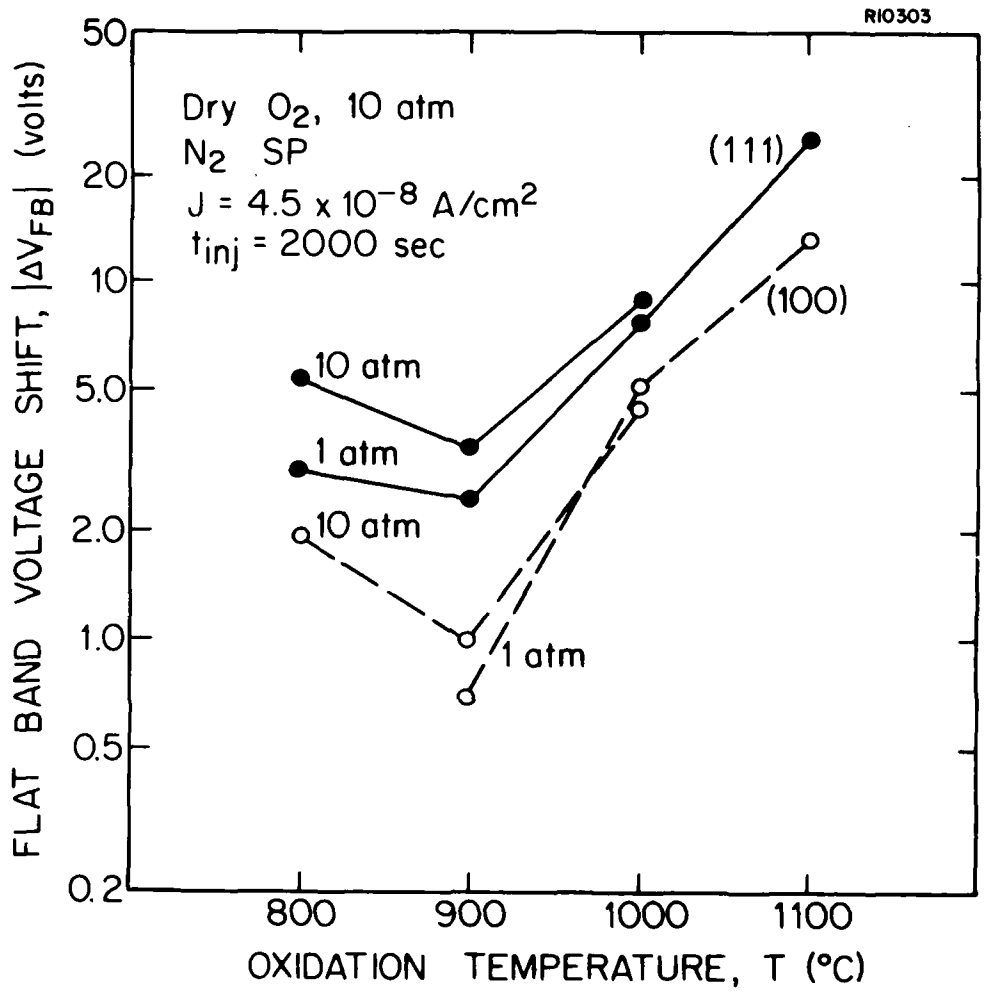

Fig. 4-12. Flat band voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (100) and (111) silicon substrates oxidized in dry O_2 at 1 and 10 atm.

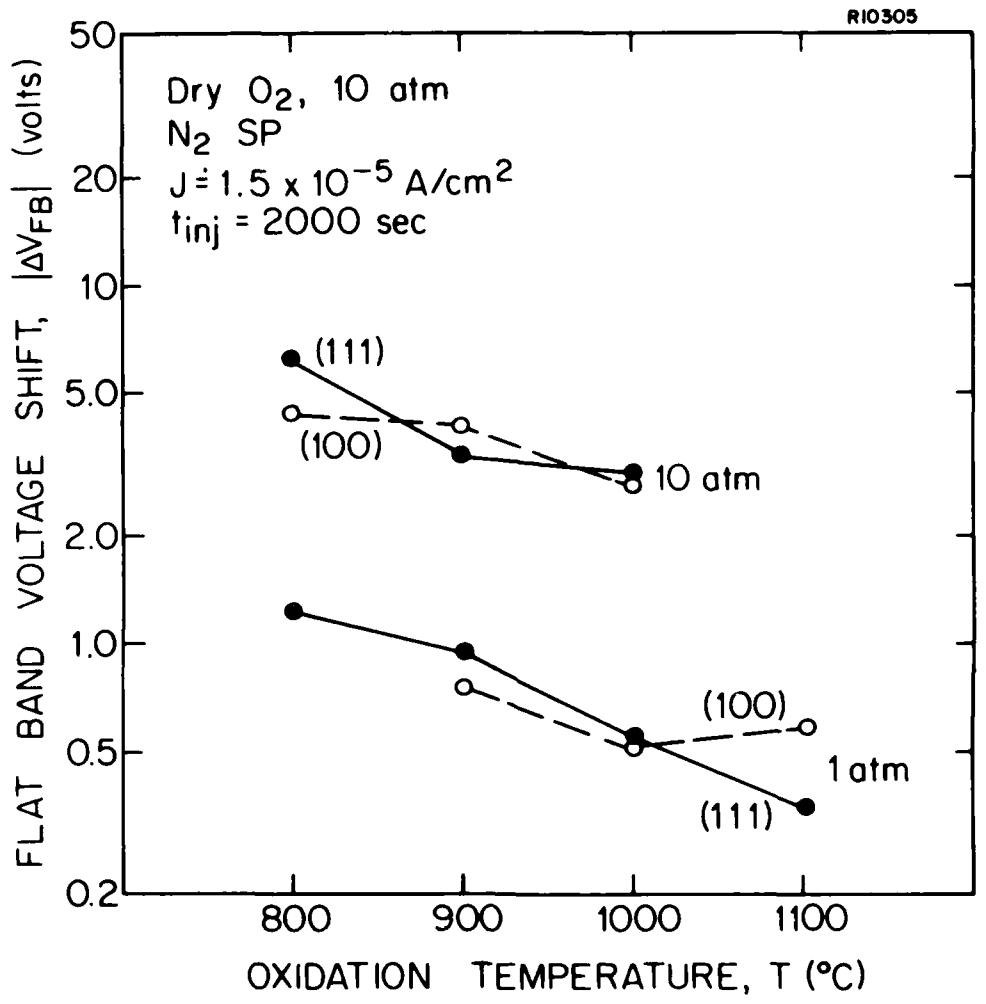

Fig. 4-13. Flat band voltage shift versus oxidation temperature for electron trapping by avalanche injection from p-type (100) and (111) silicon substrates oxidized in dry O_2 at 1 and 10 atm.

4.4.2 Hole and Electron Trapping in Steam Grown Oxides

Experiments to investigate the effect of oxidation pressure on the oxide trapped charge density N_{ot} were confined to the lowest temperature (800°C) and 5 atm. N- and p-type (100) and (111) oriented silicon wafers were used in order to measure both electron and hole trapping. The results are summarized as follows:

(a) Hole trapping measurements resulted in flat band voltage shift of 12.5 V following 2000 sec of injection time at 4.4×10^{-8} A/cm^2. This compares with 15 V for oxidation at 1 atm, 800°C and indicates no substantial increase in hole trapping due to the increased oxidation pressure.

(b) Electron trapping results are similar and indicate no substantial effect due to the oxidation pressure. Figure 4-14 shows the results at both 1 and 5 atm for p-type (111) tested at an average avalanche injection current of 1.5×10^{-5} A/cm^2. It should be noted that the characteristic shape indicative of steam oxidation is observed for both samples although they both received a post-oxidation in-situ anneal in nitrogen. An increase in anneal time may be required to reduce the trapped charge density.

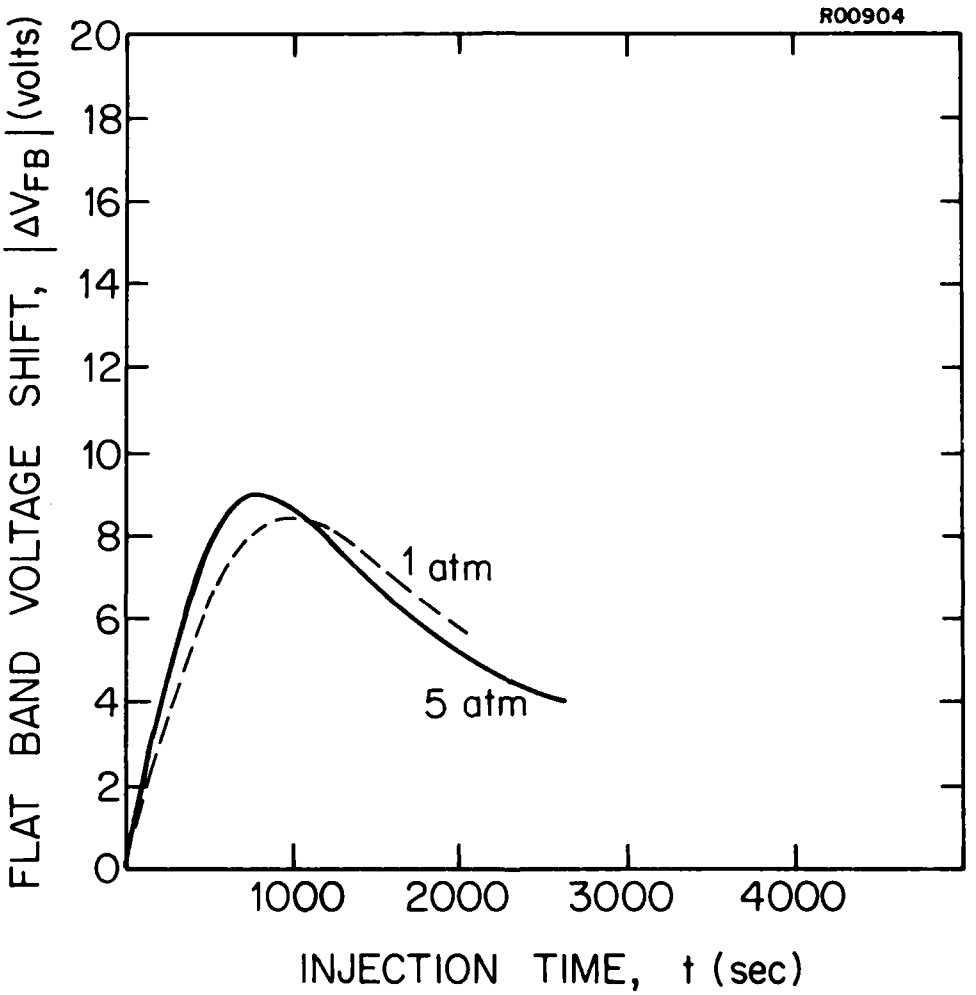

Fig. 4-14. Flat band voltage shift versus injection time for electron trapping from p-type (111) substrates oxidized in steam at 1 and 5 atm.

4.5 Hole and Electron Trapping in Poly-Si/SiO_2/Si Structures

Most fabrication procedures for MOS integrated circuits, particularly the more advanced VLSI circuits, include one or more polycrystalline silicon layers as interconnect or as a gate in an MOS capacitor or transistor structure. The possible effects resulting from the polysilicon deposition on charge trapping in the underlying oxide is a matter of considerable importance. Also critical is the degree to which the charge trapping in the oxide is dependent on the oxidation condition and the possible modification of this dependence by the polysilicon deposition step.

In some instances, such as the case shown in Fig. 4-15 for hole trapping, the deposition of poly-Si over thermally grown SiO_2 (dry O_2, ArSP) is seen as resulting in increased flat band voltage shift but retaining the general trend of greater $|\Delta V_{FB}|$ for higher temperature characteristics of argon post-oxidation in-situ anneals. This however was not typical of the remaining process conditions. Plots of flat band voltage shifts obtained for poly-Si fieldplates versus the shifts obtained when using aluminum fieldplates are shown in Fig. 4-16. Generally higher values of $|\Delta V_{FB}|$ are obtained for poly-Si fieldplates. This effect may be caused by exposure to hydrogen during the polysilicon deposition process. Such an exposure even at low temperature appears to result in increased hole trapping, as will be discussed in Section 4.7.

For electron trapping the results are quite different, as shown in Fig. 4-17. In this case, lower values of flat band voltage shifts are recorded for poly-Si than for aluminum fieldplates. The exposure to hydrogen would perhaps indicate a decrease in electron trapping sites. This result is in general agreement with that of the next section, which shows

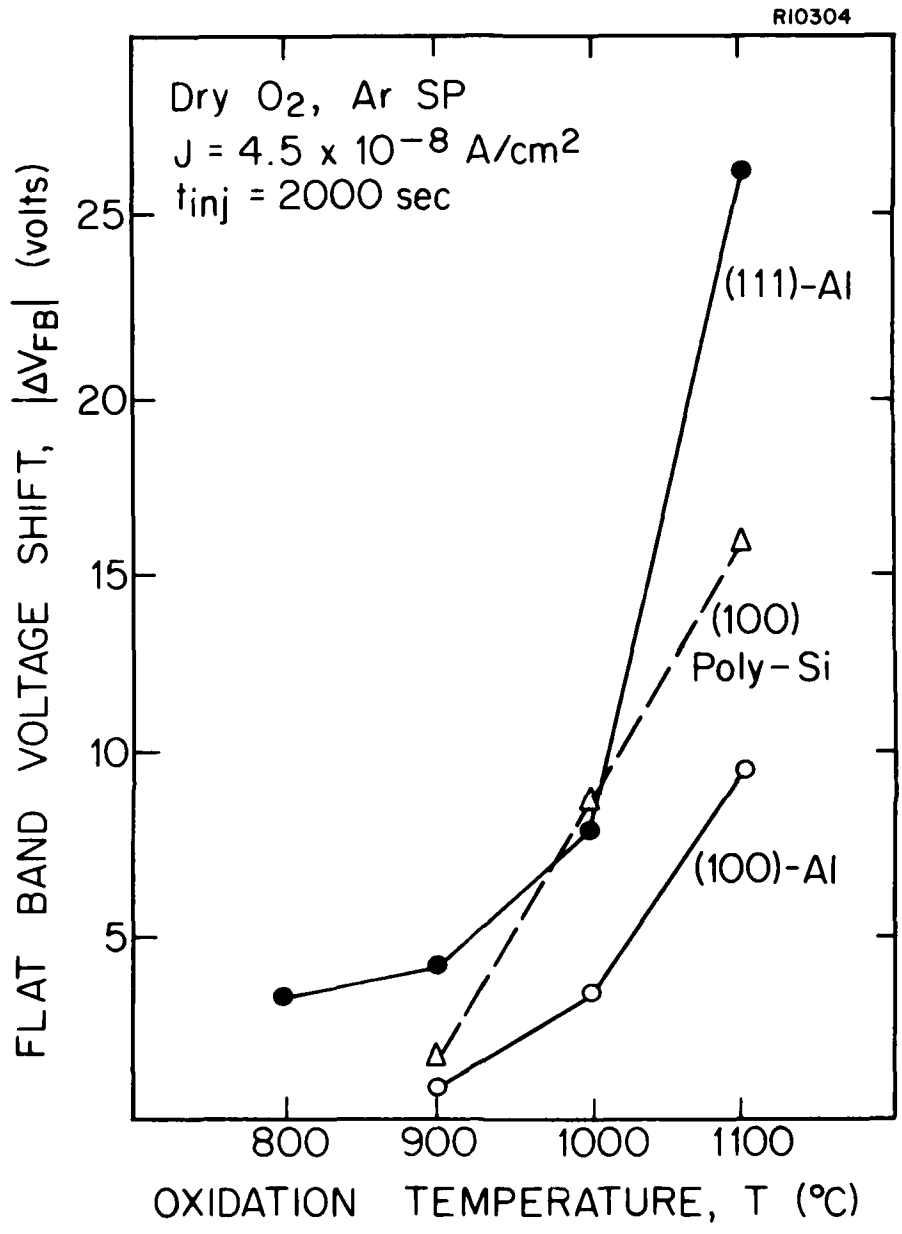

Fig. 4-15. Flat band voltage shift versus oxidation time for Al and poly-Si gated MOS structures. Wafers were oxidized in dry O_2 and annealed cooled in Ar (ArSP).

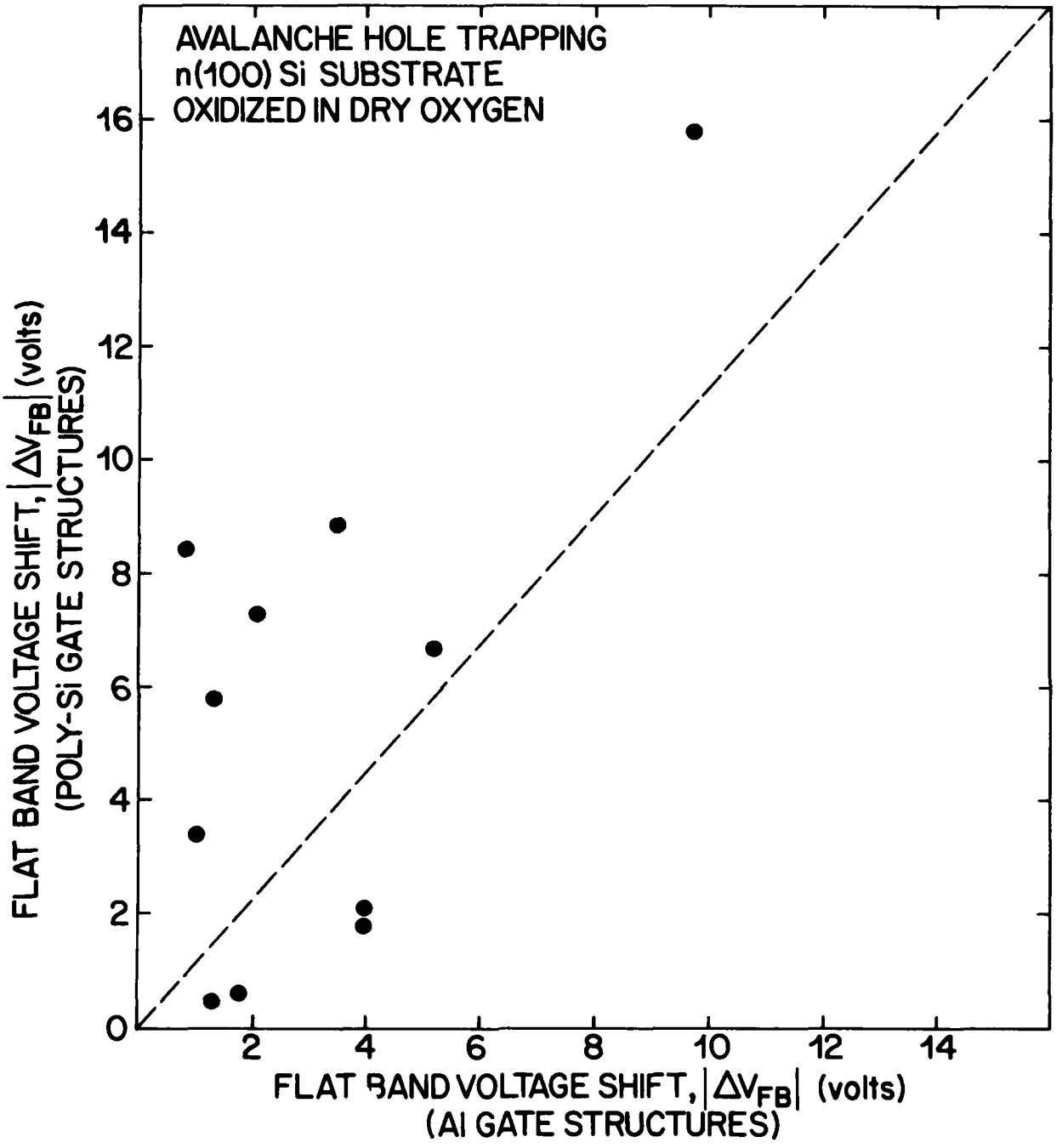

Fig. 4-16. Flat band voltage shift due to avalanche hole trapping for poly-Si gated structures versus Al gated structures.

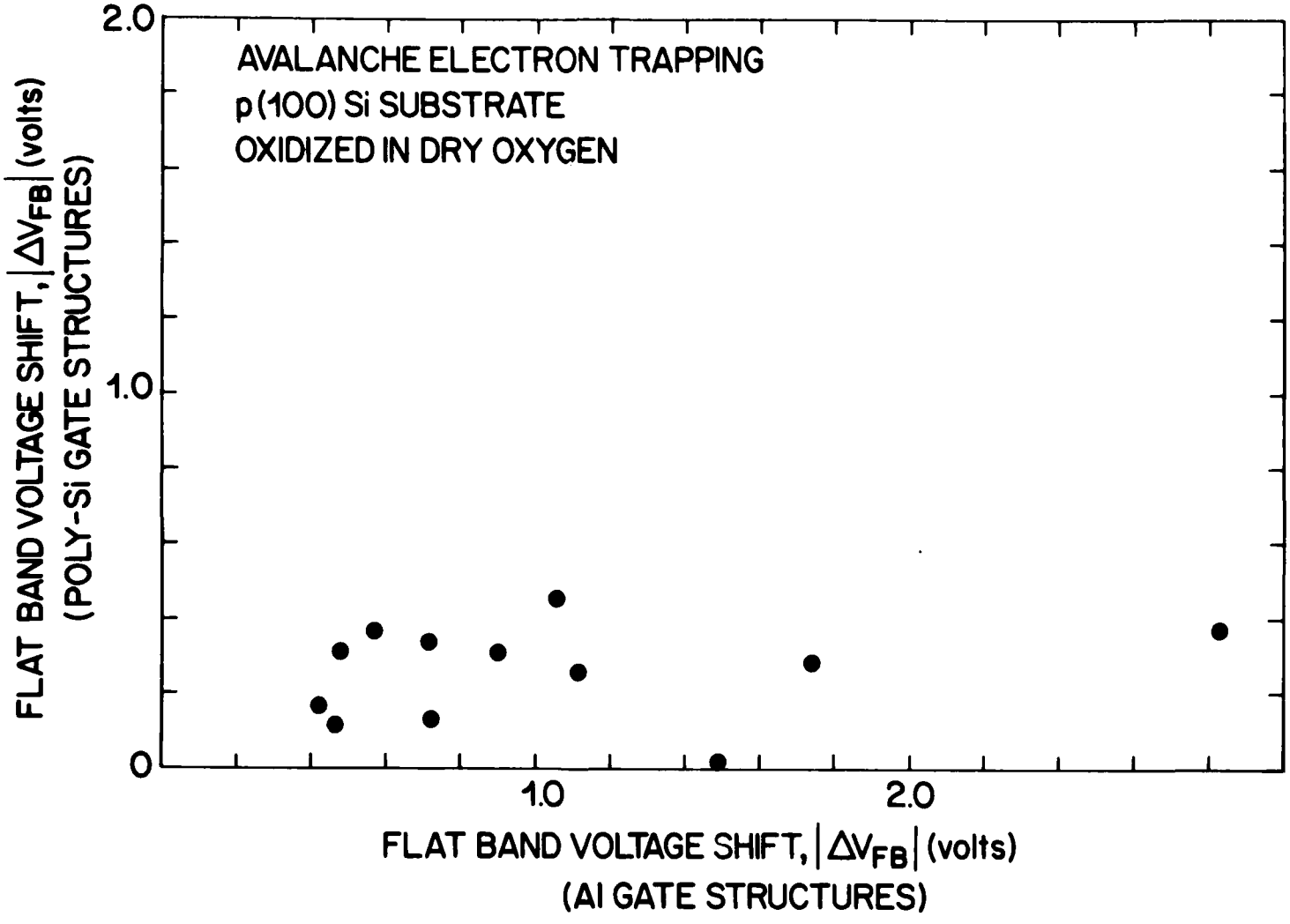

Fig. 4-17. Flat band voltage shift due to avalanche electron trapping for poly-Si gated structures versus Al gated structures.

that at lower temperatures, exposure to hydrogen does not result in an increase in electron trapping.

In summary, avalanche charge injection results using polysilicon fieldplates indicate increased hole trapping and comparable or lower electron trapping when compared to aluminum fieldplate structures. This result is attributed to the process sequence used during the polysilicon deposition cycle and is probably related to the particular ambient, temperature, time, and other parameters associated with the deposition process. A more careful examination of the variation of these parameters and their effect on charge trapping is recommended.

4.6 Effect of Low Temperature Hydrogen Anneal on Charge Trapping

The processing of MOS integrated circuits, either with metal or polycrystalline silicon gates, requires a low temperature hydrogen/nitrogen annealing step primarily to reduce the interface trapped charge density which can be detrimental to MOS transistor operation. The effect of ambient composition during the anneal has been a matter of debate as has been the role of hydrogen in enhancing charge trapping. The experiments carried out here covered three major processing sequences:

1 – Pre-metallization 100% hydrogen anneal at 400°C with no post-metallization heat treatment.

2 – No pre-metallization hydrogen treatment. Only post-metallization anneal in 100% nitrogen ambient at 400°C.

3 – Same as (2) but post-metallization anneal carried out with forming gas (10% H_2 in N_2) also at 400°C.

4.6.1 Comparison between Post-metallization Anneals

The effect of the incorporation of 10% hydrogen in the post-metallization anneal ambient at 400°C was found to have no effect on the density of trapped holes or electrons following avalanche injection. This result is somewhat unexpected in view of results published in the literature which indicate a detrimental effect due to exposure to hydrogen. In this case, however, since the annealing is thought to occur due to the creation of active hydrogen by the interaction between the Al fieldplate and moisture resulting in the system, and this reaction can occur in a 100% nitrogen ambient, the addition of 10% hydrogen has no effect on the annealing of interface traps, and from our results here has no effect on the trapping properties of the film.

Figure 4-18 shows a representative plot of flat band voltage shifts due to hole trapping obtained for samples processed simultaneously with only the post-metallization anneal being different. The results indicate clearly that the variations are within experimental errors and that there is no difference between the two annealing procedures.

4.6.2 Comparison between Pre- and Post-metallization Anneals

The role of hydrogen is further examined by comparing samples that received a pre-metallization 100% hydrogen anneal with those receiving the post-metallization anneal. The interest in annealing the structures without fieldplates in 100% hydrogen stems from the fact that most IC devices no longer have metal fieldplates and that exposure to a more concentrated hydrogen ambient for longer time periods is often

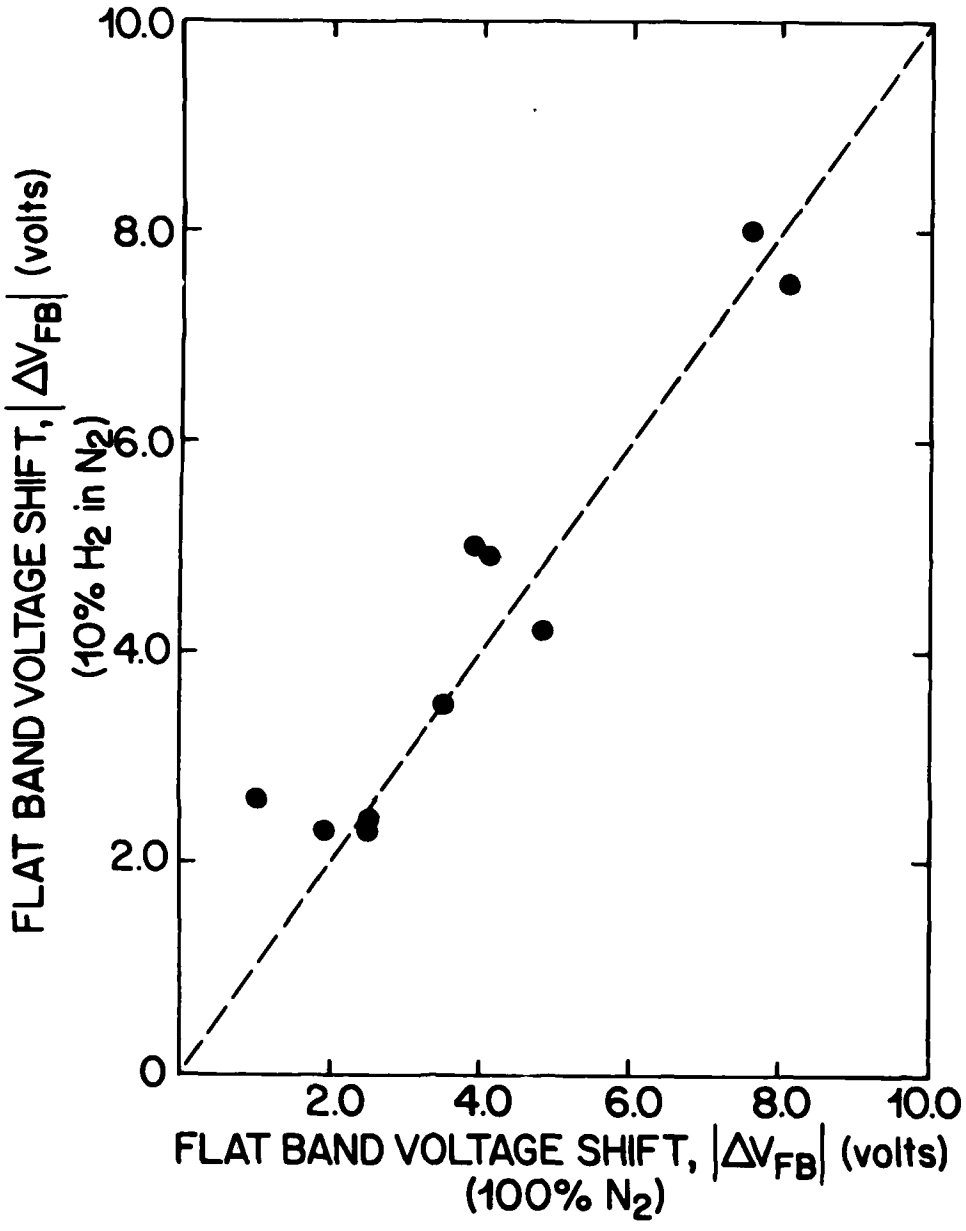

Fig. 4-18. Effect of post-metallization anneal on flat band voltage shift.

necessary to reduce the density of interface states or traps. Typical results for hole and electron trapping are shown in Figs. 4.19 and 4.20 respectively.

In the case of hole trapping, it is quite clear that a pre-metallization anneal in hydrogen results in increased hole trapping for both (100) and (111) substrates, and for dry and steam oxidation, at atmospheric and higher pressures. Surprisingly, for electron trapping the difference appears much smaller and only at higher flat band voltage shifts does it clearly appear that the pre-metallization anneal results in increased electron trapping.

In summary, low temperature hydrogen treatments appear to have a significant effect on hole trapping only when the oxide is exposed to a 100% hydrogen ambient without a metal fieldplate. In all other cases investigated the effect is small or negligible.

4.7 Trapping in Oxides Exposed to Process Related Radiation

Several processing steps used in the fabrication of advanced integrated circuits require the sample to be exposed to radiation such as electron beams, x-rays, laser beams, and others. A summary of some of these processes is shown in Fig. 2-2. In this section we present results obtained in the investigation of the following processes:

(a) Exposure to an electron beam during lithography for the purpose of forming small-scale device structures.

(b) Exposure to an electron beam following an ion implantation for the purpose of annealing the implant damage and activating the dopant.

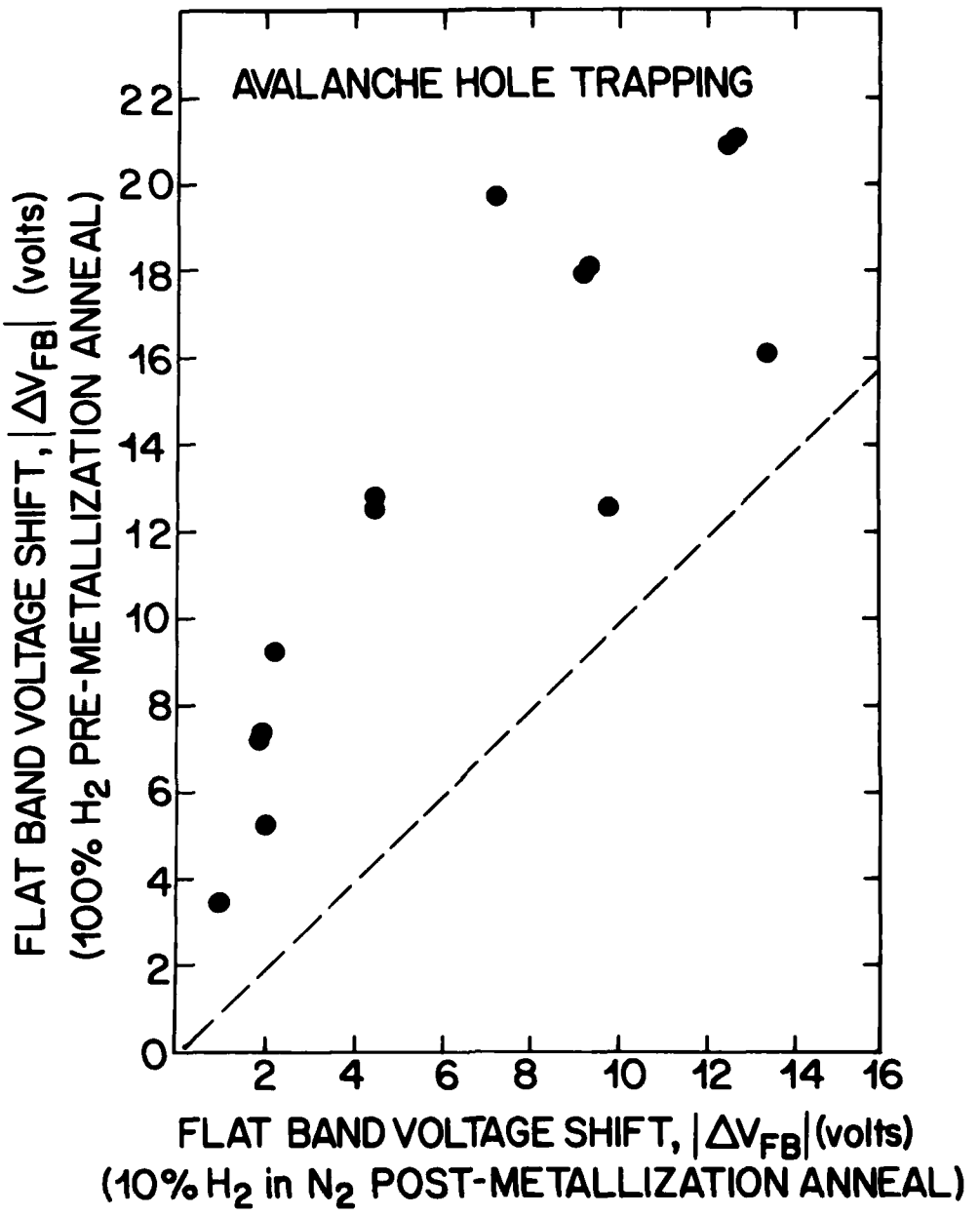

Fig. 4-19. Flat band voltage shift due to hole trapping for pre-metallization annealed samples versus post-metallization annealed.

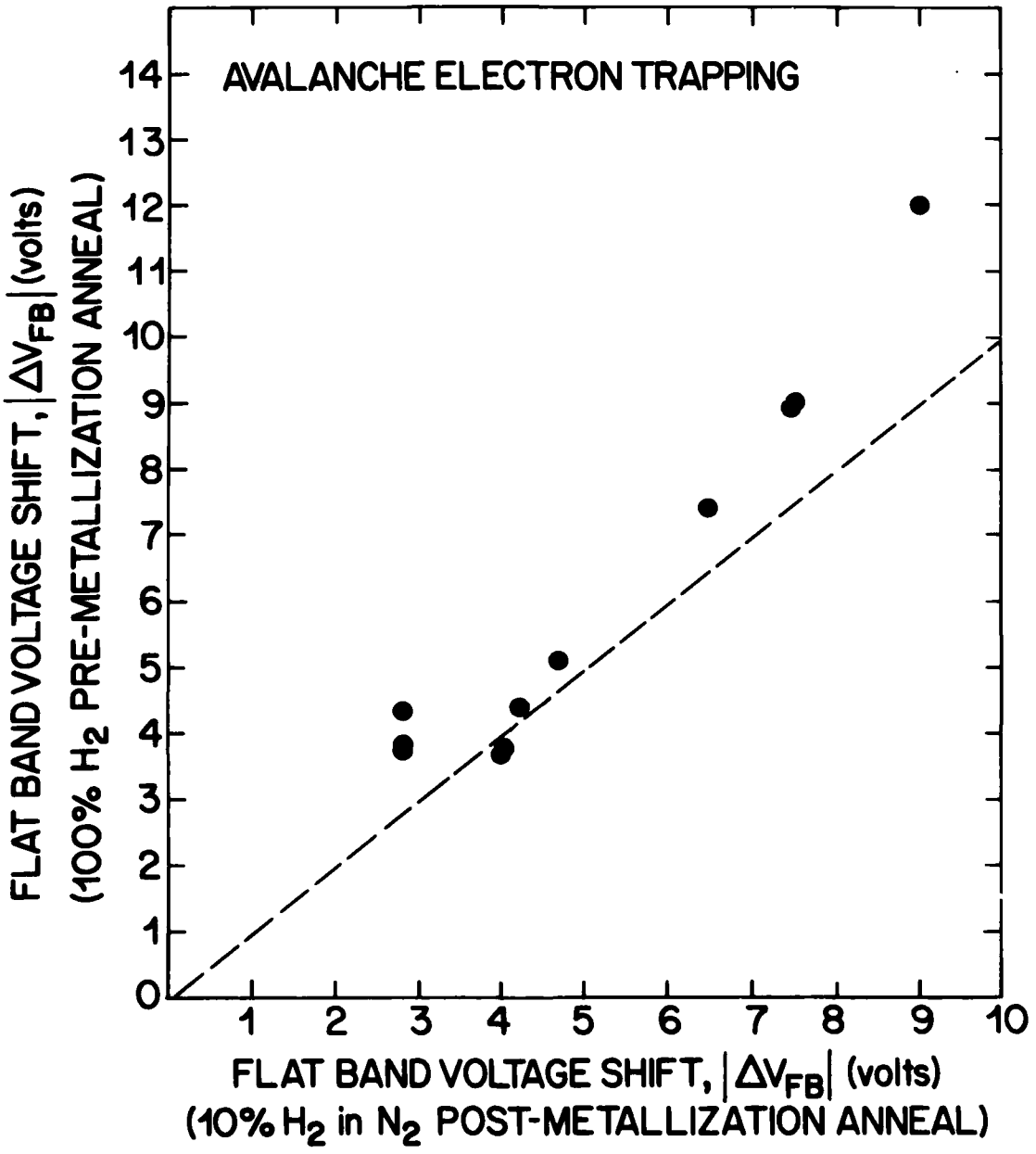

Fig. 4-20. Flat band voltage shift due to electron trapping for pre-metallization annealed samples versus post-metallization annealed.

(c) Exposure to a laser beam for the same purpose outlined in (b).

(d) Exposure to radiation during ion implantation. This process is commonly used in most advanced VLSI circuits and the effect of implantation on the oxide charges and traps is quite important.

4.7.1 Exposure to Electron Beam (Lithography Dose $\doteq 10^{-4}$ C/cm^2)

N- and p-type (100) silicon wafers of resistivity 0.2-0.3 and 0.4-0.7 Ω-cm respectively were used to investigate the effects of electron beam exposure on fixed oxide charge (N_f), interface trapped charge (N_{it}), and oxide trapped charge (N_{ot}). All electron beam exposures were carried out by Dr. R. Fabian Pease at Stanford University. The process and measurement sequence is outlined below:

1 – Wafers were oxidized in dry O_2 or steam at 1000°C and received a post-oxidation in-situ anneal in argon for 10 min. The oxidation was followed by a cool in argon (ArSP) for dry O_2 oxidation and no anneal for steam oxidation (H_2OP).

2 – Metal was cold flash evaporated and 750 μm dots formed by conventional photolithography.

3 – The wafers were annealed at 400°C in forming gas (10% H_2 in N_2) for 20 min.

4 – Parts of each wafer were irradiated with a 10^{-4} C/cm^2 electron beam. One half of each wafer was shielded from the electron beam with a dummy silicon wafer. The remainder of each wafer was exposed to scattered electrons, as shown in Fig. 4-21(a).

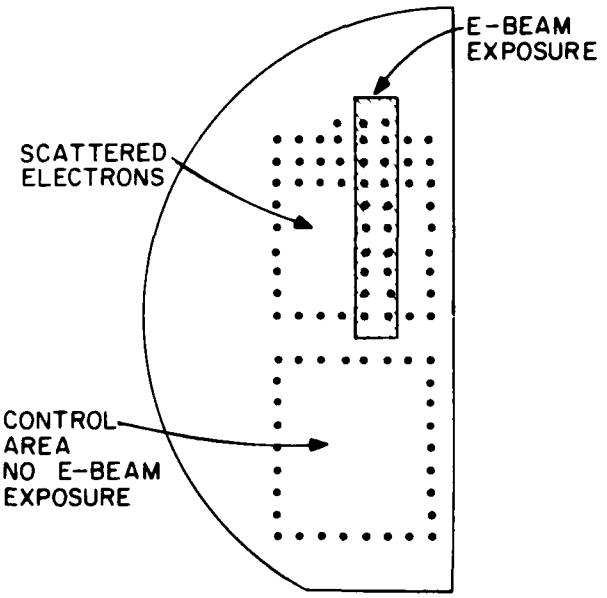

Fig. 4-21(a). E-beam exposure on test wafers was carried out according to the above pattern.

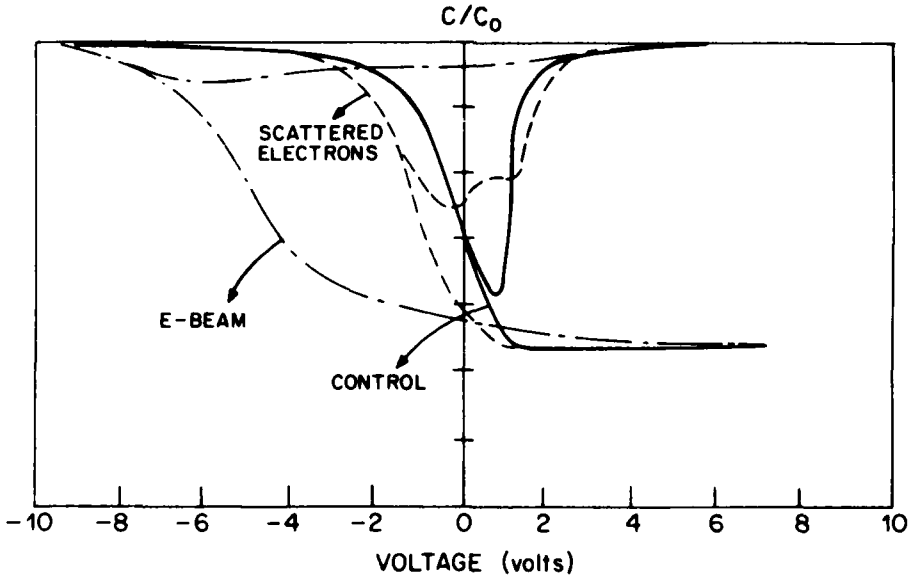

Fig. 4-22(b). High frequency and quasistatic C-V curves for MOS structures on p-type (100) silicon. The capacitors were exposed to electron irradiation following a post-metallization anneal.

5 – Wafers were annealed either at 400°C or 500°C in forming gas for 20 min.

6 – Electrical measurements were performed in order to measure effective fixed oxide charge (N_f), interface trapped charge (N_{it}), and oxide trapped charge (N_{ot}) densities at the various locations on the wafer.

Following wafer irradiation (step 4) and prior to wafer anneal (step 5), the high frequency and quasistatic C-V curves were measured and the results shown in Fig. 4-21(b). Areas directly exposed to the electron beam or to scattered electrons showed shifts in both V_{FB} and V_{TH} indicating hole trapping and generation of interface states. This is expected from any radiation exposure. The annealing performed in step 5 was carried out to investigate whether N_f, N_{it}, and N_{ot} could be annealed out either at 400°C or 500°C. Of considerable importance is the possible generation of neutral traps which would not respond to the anneal cycle. These neutral traps can only be observed with post-anneal carrier trapping measurements.

A summary of the results obtained is shown in Figs. 4-22 through 4-26. Effective fixed oxide charge densities for both n- and p-type wafers are shown in Fig. 4-22 for all three regions of each wafer. Data indicate minimum contribution to fixed oxide charge resulting from the electron beam exposure. Most of the variations noted are a result of pre- and post-electron beam processing and are essentially uniform throughout the whole wafer.

Figure 4-23 summarizes the interface trapped charge data in a similar manner. No evidence of residual interface traps specifically associated with the electron beam exposure can be detected.

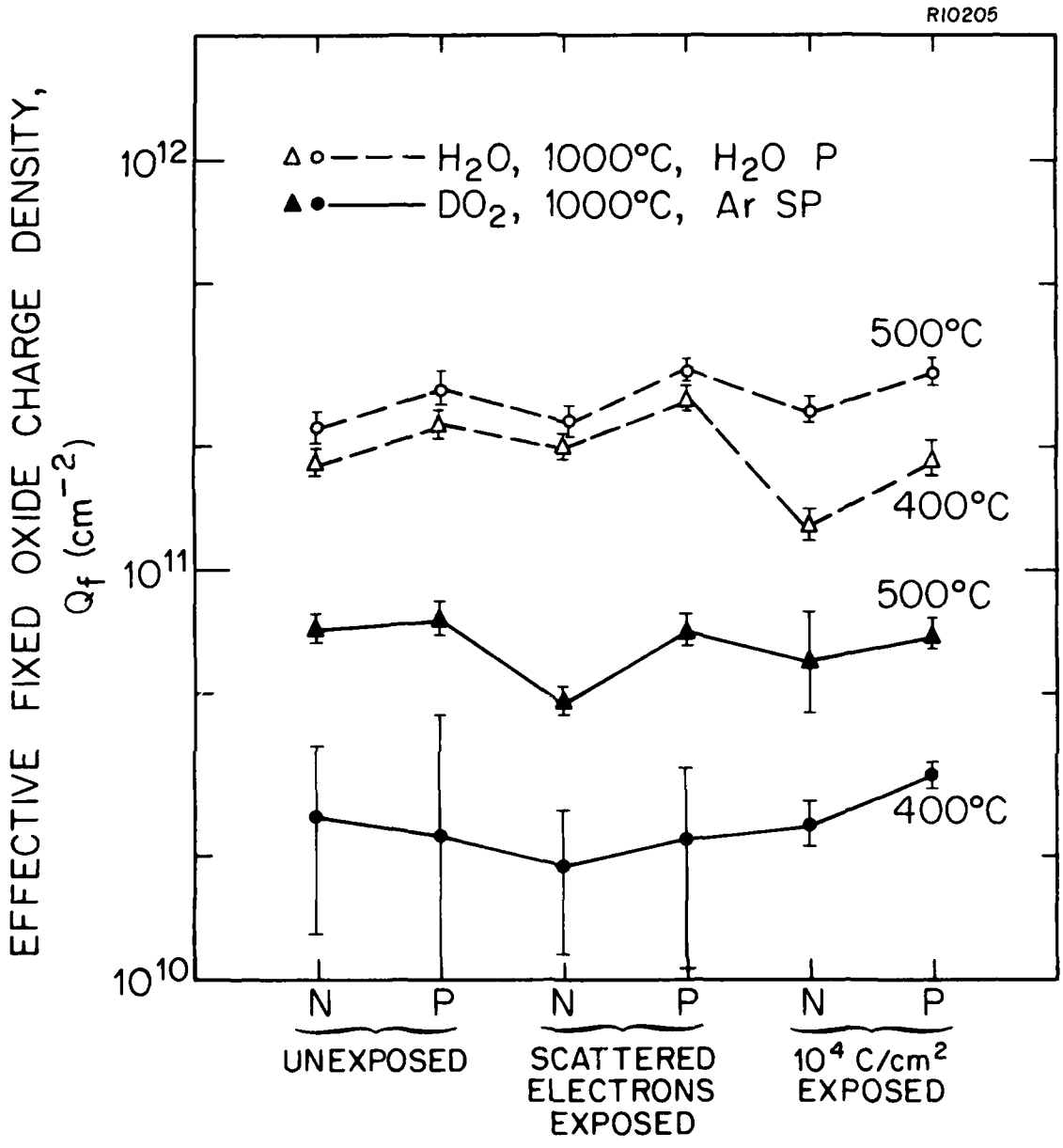

Fig. 4-22. Effective fixed oxide charge density for MOS capacitor structures exposed to an electron beam (10^4 C/cm^2 @ 20 kV). Both p- and n-type wafers were used and three areas on each wafer evaluated: (a) exposed to 10^4 C/cm^2 electron beam; (b) exposed to scattered electrons only; (c) covered during exposure.

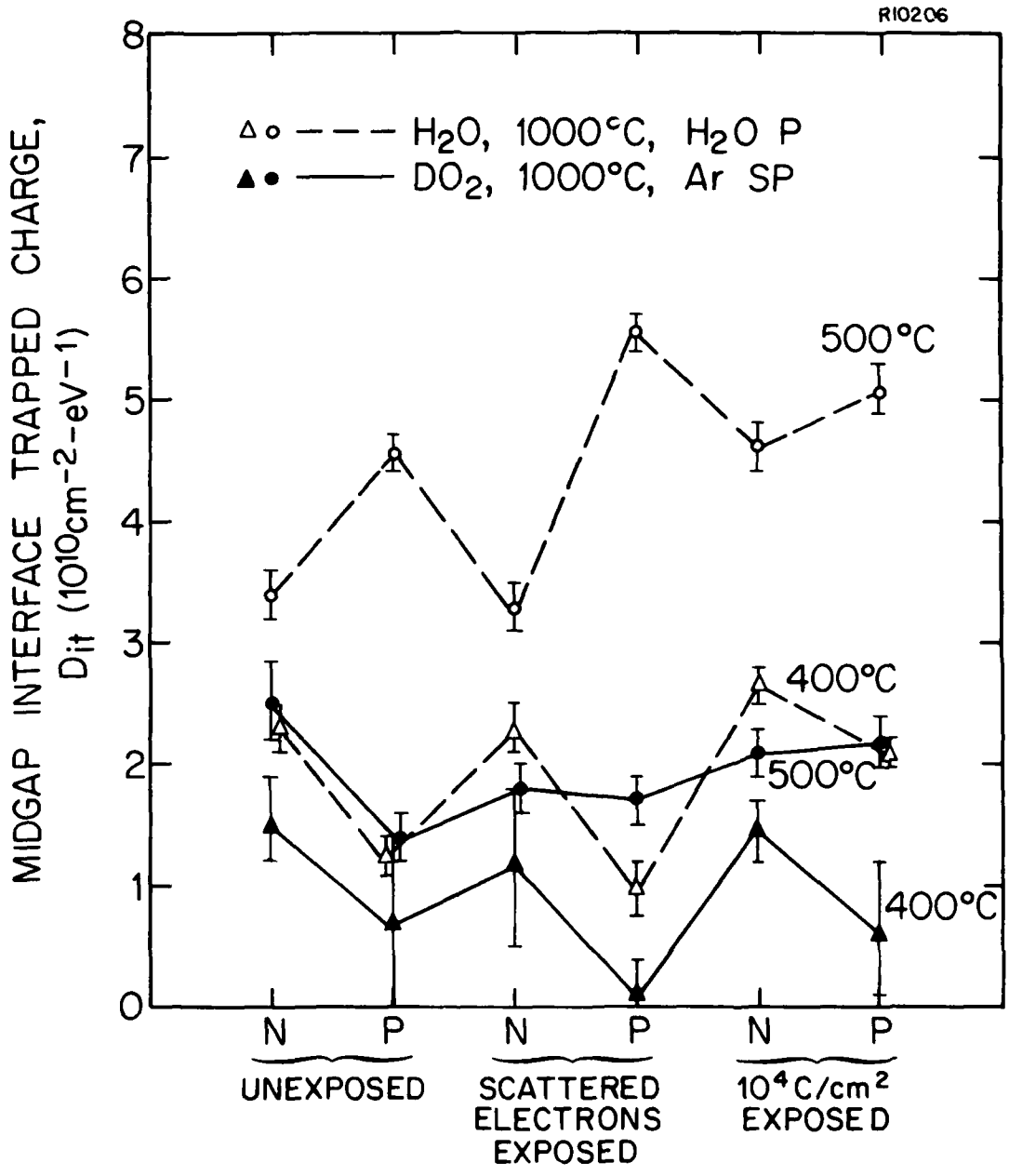

Fig. 4-23. Interface trapped charge density at midgap for the same MOS structures of Fig. 4-22.

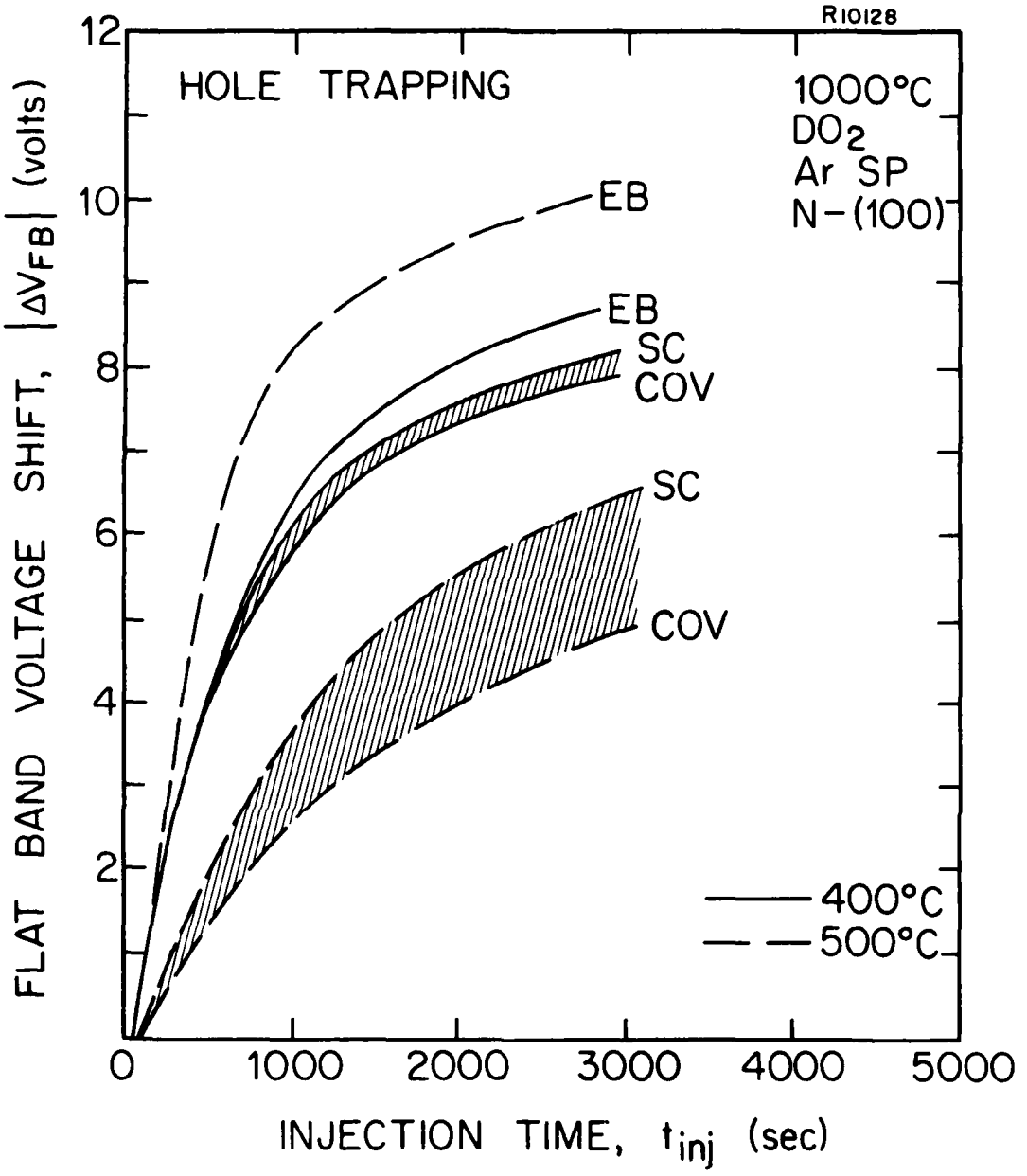

Fig. 4-24. Flat band voltage shift versus hole injection time at an average current of 4.4×10^{-8} A/cm^2. The wafers were oxidized in dry O_2 and annealed/cooled in argon at 1000°C. Following E-beam exposure 10^4 C/cm^2) the wafers were annealed in 10% H_2 in N_2 for 20 min at 400°C or 500°C. COV = Covered – no E-beam exposure; SC = Exposure to scattered E-beam; EB = E-beam direct exposure.

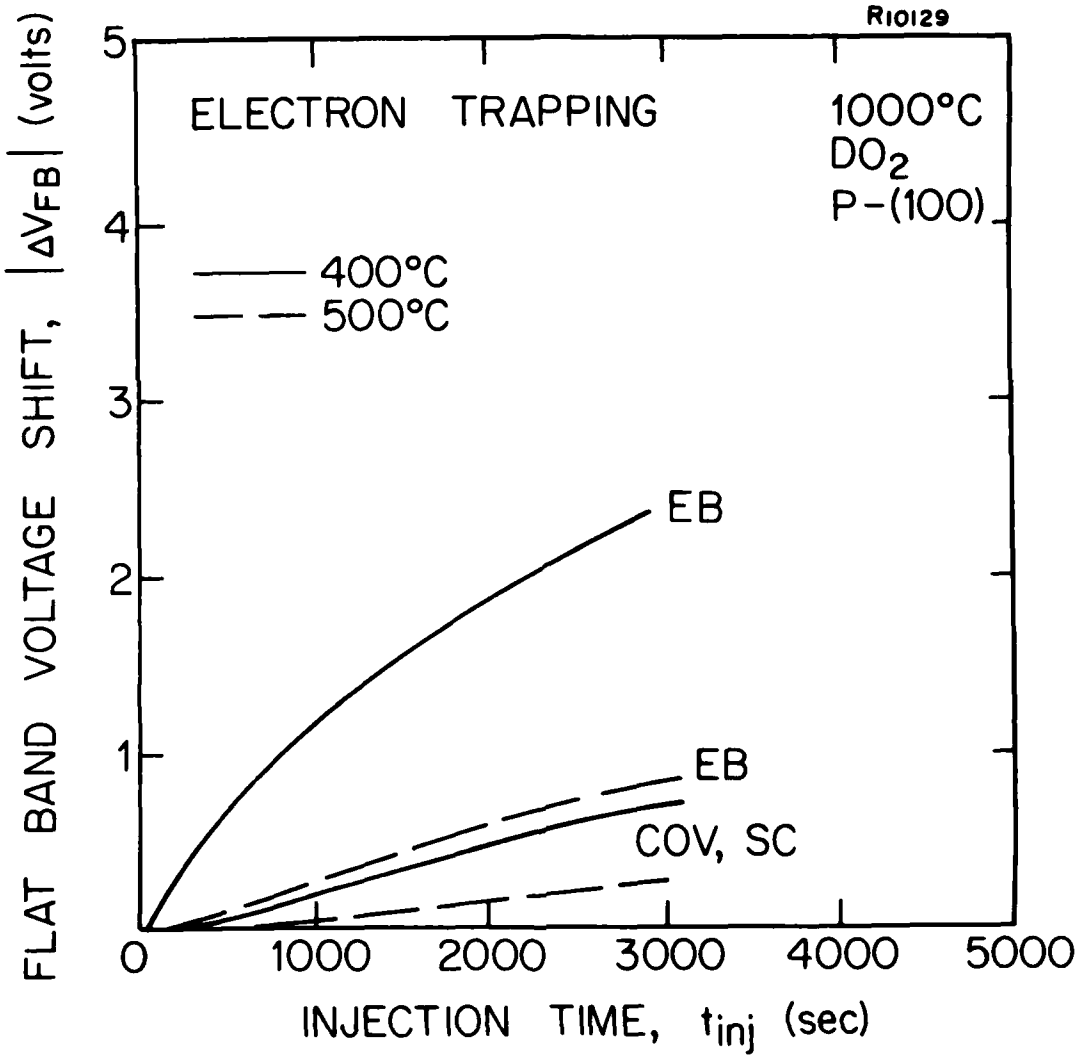

Fig. 4-25. Flat band voltage shift versus electron injection time at an average current of 1.5×10^{-5} A/cm^2. All other parameters are the same as Fig. 4-24.

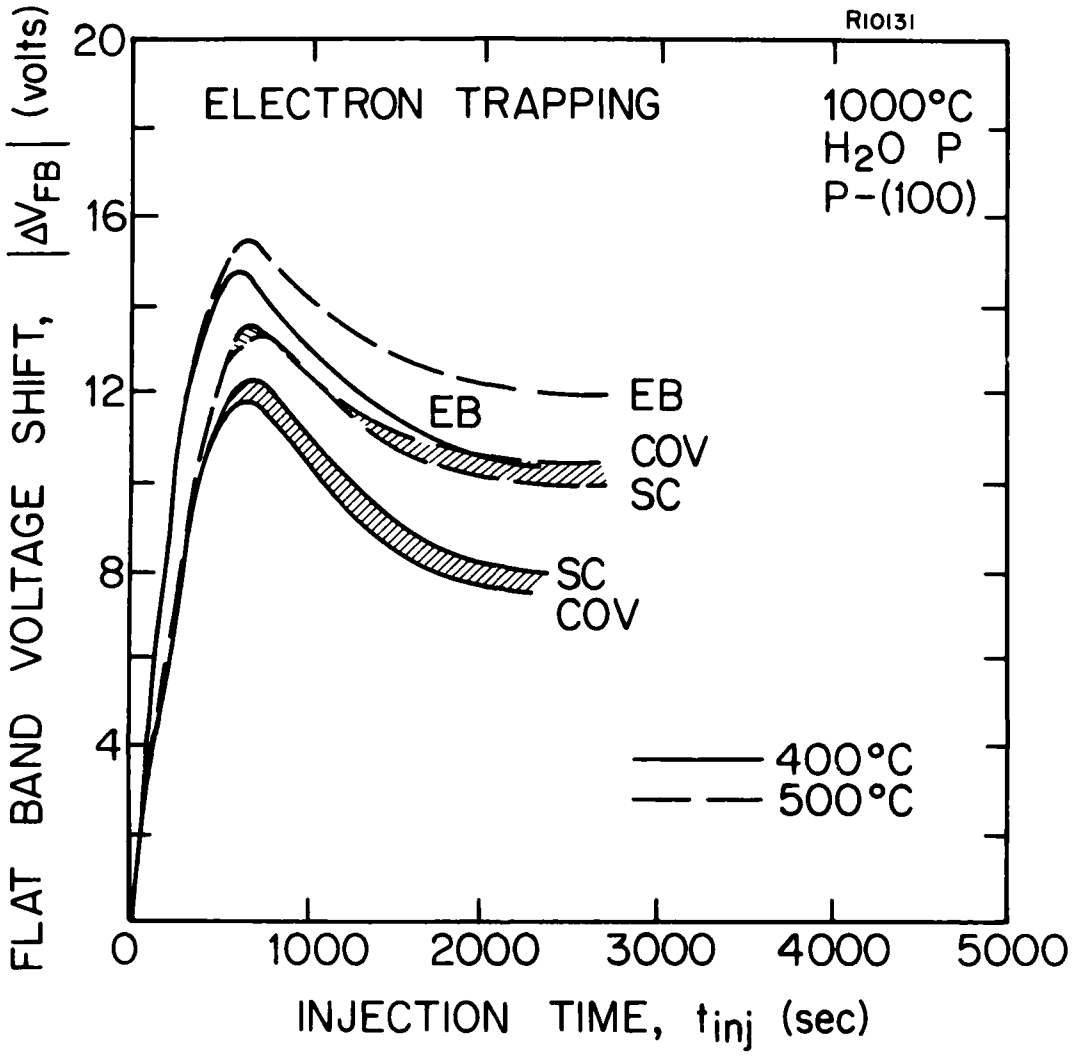

Fig. 4-26. Flat band voltage shift versus electron injection time at an average current of 1.5×10^{-5} A/cm^2. The wafers were oxidized in pyrogenic steam at 1000°C and cooled in the oxidizing ambient. Other processing parameters are the same as Fig. 4-24.

Figures 4-24 to 4-26 represent flat band voltage shifts due to avalanche charge injection of holes and electrons. The amount of shift is related to both the densities and cross sections of the traps. The data indicate an increase of up to 100% in the flat band voltage shift resulting from the electron beam exposure. It should be noted though that the percentage increase is related to the processing history of the sample and the nature of the traps (holes or electron traps). In Fig. 4-26 the N-shaped curve typical of electron trapping in steam grown oxides is evident and the electron beam exposure effect is also clear. The results of Figs. 4-24 to 4-26 coupled with results from Figs. 4-21 and 4-23 indicate that electron beam exposure will result in neutral trap formation. Some of these traps are unannealable at 400-500°C and could result in device degradation in cases of hot electron injection and ionizing radiation exposure. The traps are, however, process dependent, as was shown in previous sections, and their effect can be minimized by proper processing prior to as well as subsequent to electron beam exposure.

4.7.2 Exposure to Electron Beam (Damage Anneal Dose $0.39\text{-}3.1 \times 10^{-2}$ C/cm^2)

In recent years, laser and electron beams, both pulsed (44-46) and cw (47-50), have been used to anneal ion implant damage in silicon. Furthermore, specific devices such as diodes, bipolar transistors and MOSFETs have been fabricated using these techniques in place of a conventional furnace anneal.

The energy transfer achieved by scanning cw laser or electron beams results in localized heating of the implanted area which when coupled with the small exposure time can result in nearly total dopant activation and lattice damage

anneal with practically no dopant redistribution (49,51). Electron beam annealing offers the advantage of being free of the optical interference resulting from varying oxide thicknesses which make laser annealing dependent on surface conditions. In some cases, this dependence on surface conditions can be used advantageously to achieve selective annealing.

A major concern that arises when considering the use of electron beam annealing in MOS device fabrication is the damage to thin gate oxides which might cause undesired device instabilities. Kamins and Rose (46) have noted distorted and shifted high frequency C-V curves after pulsed electron beam annealing. These curves returned to their pre-exposure form following a standard low temperature hydrogen anneal. This is the same as the behavior reported in Section 4.8.1 and in Figs. 4-22 and 4-23. The generation of neutral traps which are unannealable is observable by means of avalanche charge injection or any similar technique for charge generation and trapping. The effect observed in Section 4.8.1 suggests that electron beam exposure at the higher doses investigated here will undoubtedly result in increased trapping of both electrons and holes.

Oxides were grown 800 Å thick in dry O_2 at 1000°C on n- and p-type (111) silicon substrates of resistivity 0.2-0.3 and 0.4-0.7 Ω-cm respectively.

Oxides were then exposed to a scanned electron beam at Varian Associates Inc. by Drs. R. T. Fulks, R. A. Powell, and T. O. Yep in a system which has recently been described (52). This system uses a large-area scanned e-beam and operates in the isothermal dwell mode where dwell times are 5-10 sec and the entire bulk wafer is heated. No substrate heating is required and anneals are done in vacuo ($\sim 10^{-5}$ torr). A constant power of 5 kV, 50 mA was applied to a 12.5 × 50 mm area by

defocusing the 6 mm diameter incident beam and scanning in one direction at a frequency of 25 Hz. Exposure time was changed by moving the sample at different speeds under the slit of electrons and the fluence was varied from 0.39 to 3.10×10^{-2} C/cm^2. The higher fluences are typical of those used for isothermal annealing of ion implant damage. It is noted that the incident electron charge densities used in this experiment are somewhat higher than those used for pulsed e-beam annealing (1×10^{-4} C/cm^2 for a 20 keV, 100 nsec, 2 J/cm^2 pulse) but comparable to cw scanned systems which focus to small spots ($\sim$50 μm) and use short dwell times ($\sim$3 msec). These exposures are also two or three orders of magnitude higher than those used for e-beam lithography.

Oxide charge measurements were carried out on MOS capacitor structures formed on n-type (111) silicon substrates and exposed to various scanning electron beam fluences. Results shown here have also appeared in a separate publication (53). Effective oxide charge density N_{eff}, which is shown in Fig. 4-27, contains contributions of both interface traps (N_{it}) and oxide trapped charge (N_{ot}) as well as fixed oxide charge (N_f) as a function of electron beam fluence in the range of 0.39 to 3.10×10^{-2} C/cm^2. One half of each wafer was used as a control to ensure the validity of the results. Following a 15 minute anneal in forming gas (10% H_2 in N_2) at 400°C, the effective oxide charge density is seen increasing steadily with electron beam fluence. An additional 30 min anneal in forming gas results in a decreased charge density in both the electron beam and the control wafers, primarily reflecting a decrease in interface traps due to the longer hydrogen anneal. The oxide charge resulting from the beam exposure is still not reduced to the control level and is clearly unannealable at 400°C. A third annealing treatment at 500°C yielded a similar result, although higher densities of charges were obtained due to the higher anneal temperature.

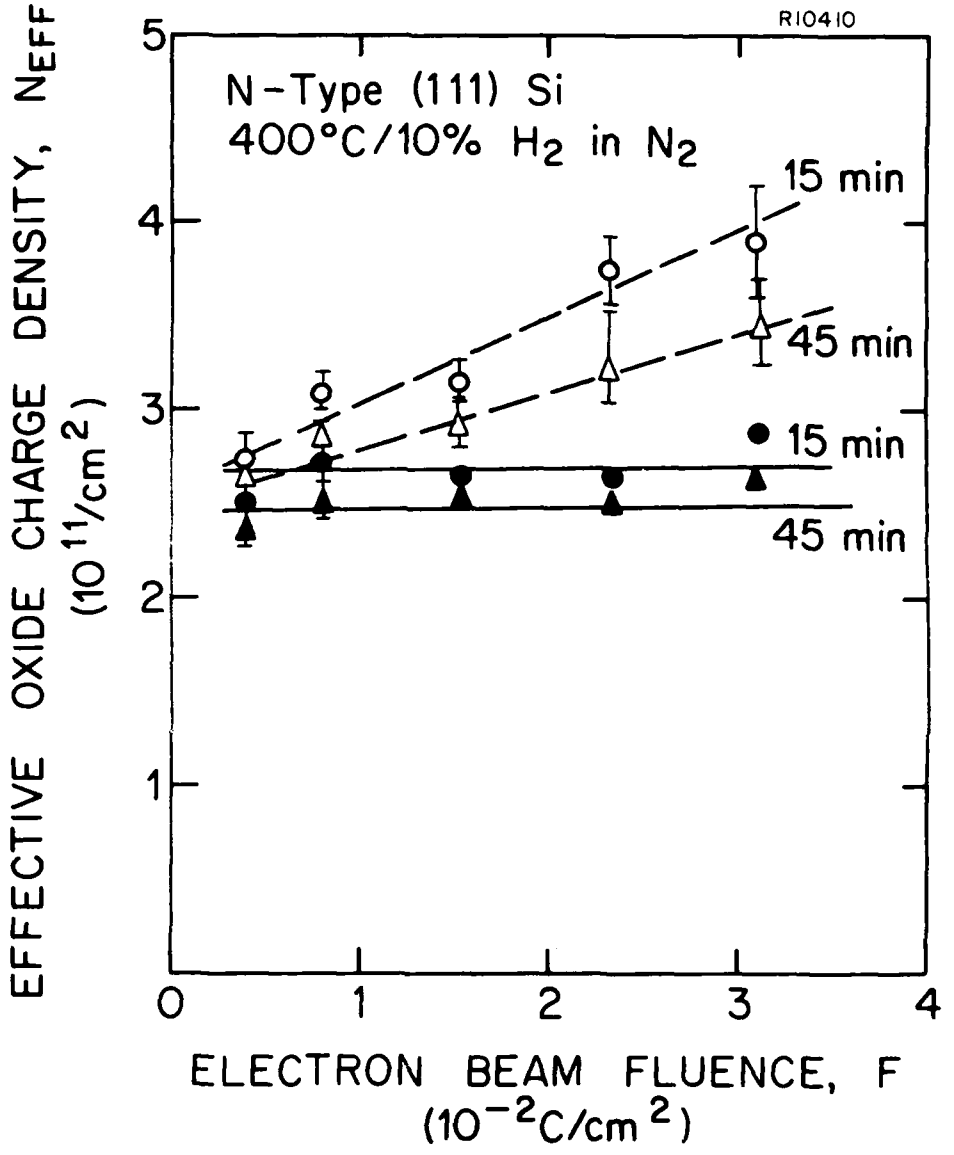

Fig. 4-27. Effective oxide charge density versus electron beam fluence. Following exposure the wafers were annealed for 15 and 45 min in forming gas at 400°C (●▲ controls; o△ irradiated).

Figure 4-28 illustrates the variations in interface trapped charge density at midgap as obtained from quasi-static C-V measurement. Data following a 45 min anneal at 400°C only are shown for clarity. Interface trapped charge density for e-beam irradiated oxides was not reduced to the control level following anneal in forming gas. However, these levels of interface charge density are considered acceptable for VLSI device fabrication. For forming gas anneals carried out at higher temperatures (500°C), N_{it} increases for both the control and the irradiated wafers.

Avalanche charge injection measurements were carried out to determine the amount of charge trapping in the electron beam irradiated oxides. The measurement would also determine whether irreversible damage occurred through the generation of trapping centers that are not annealable at 400-500°C in forming gas.

In the case of electron trapping, unexposed areas yielded flat band voltage shifts of less than 1 V following 2000 sec of injection time at 1.5×10^{-5} A/cm^2. This is in agreement with the results of Section 4.1.2 and Fig. 4-4. Following exposure to the scanning electron beam flat band voltage shifts of 9-24 V, depending on dose, were measured. However, a clear dose dependence could not be ascertained in the dose range tested, 0.39 to 3.1×10^{-2} C/cm^2.

Hole trapping measurements on unexposed control wafers yielded flat band voltage shifts of about 8 V at 2000 sec and 4.4×10^{-5} A/cm^2. This result is in agreement with previously obtained data in Section 4.1.1 and Fig. 4-2. Following electron beam exposure, the flat band voltage shift doubled to 16 V.

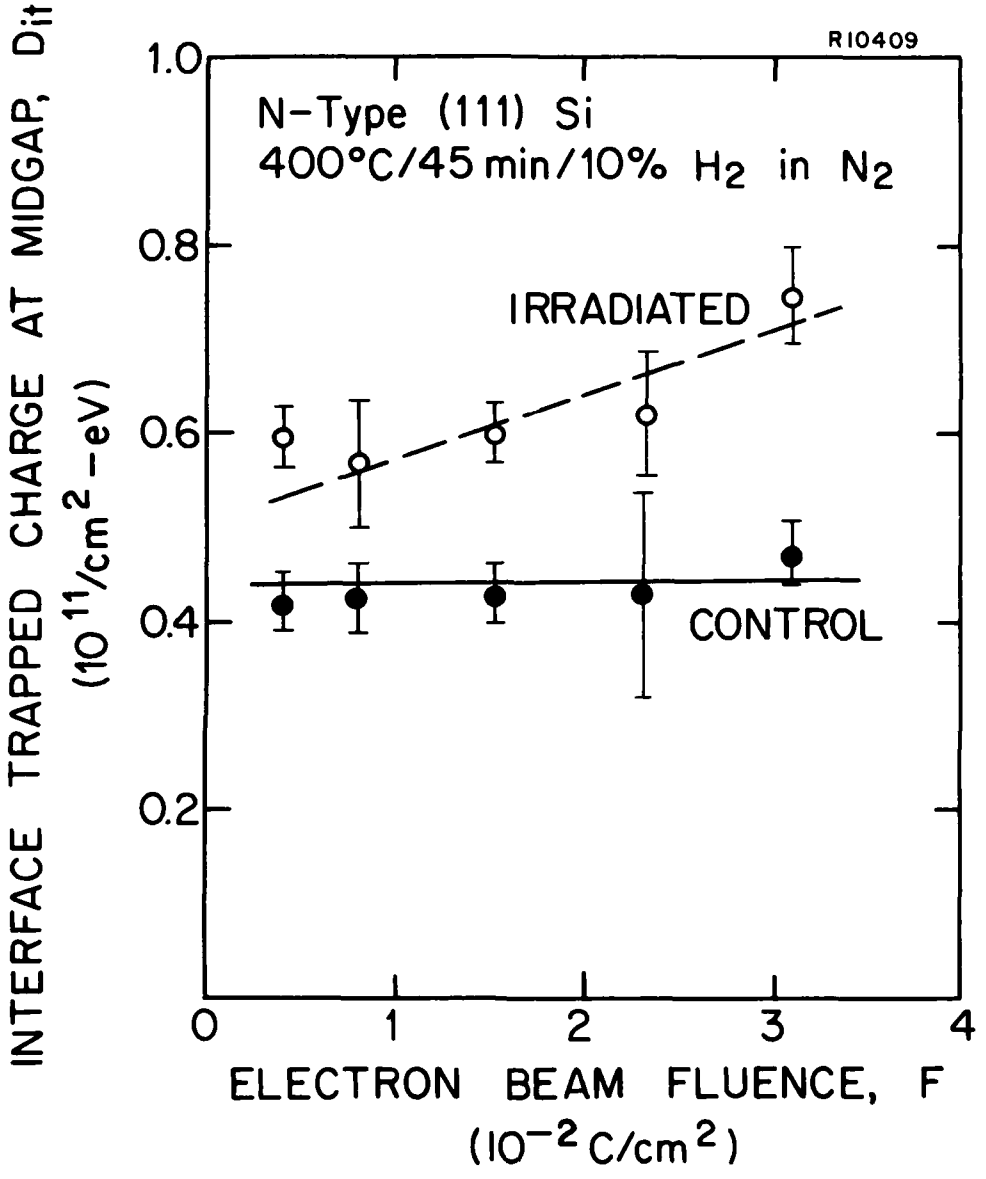

Fig. 4-28. Interface trapped charge density versus electron beam fluence for n-type (111) silicon structures annealed following exposure and metallization in forming gas at 400°C for 45 min.

Figure 4-29 shows flat band voltage shift versus injection time for both electron beam exposed and control wafers. The figure illustrates the substantial increase in effective trap density, particularly in the case of electron traps, due to the electron beam.

Both electron and hole trapping results indicate that potentially serious problems may arise if scanned cw electron beams are employed for the anneal of ion implantation damage and electrical activation of the implanted dopants. The oxide trap generation is most likely the result of bond disruption near the oxide-silicon interface or in the oxide bulk caused by collisions with the incident 5 kV electrons and lower energy secondary electrons, or by x-rays generated near the silicon interface. One possible alternative annealing approach would involve the use of scanning electron beams from the backside of the wafers. Because a 5 kV electron beam penetration and associated x-ray generation and absorption in silicon is limited to depth of less than 5 μm, this method should not produce significant charge trapping in the topside oxide. Measurements carried out on wafers exposed to electron beams through the backside did not show a meaningful increase in flat band voltage for either hole or electron avalanche injection.

4.7.3 Exposure to Laser Beam

Laser exposure was performed at Fairchild research and development laboratories by Dr. M. Delfino, with the cw multiline output (weighted wavelength average of 0.496 μm) of an Ar-ion laser. The beam was focused onto the sample with a 100 mm focal length achromatic lens to a spot size of about 35 μm. The sample was held by a copper vacuum chuck mounted on a computer-controlled x-y translation stage.

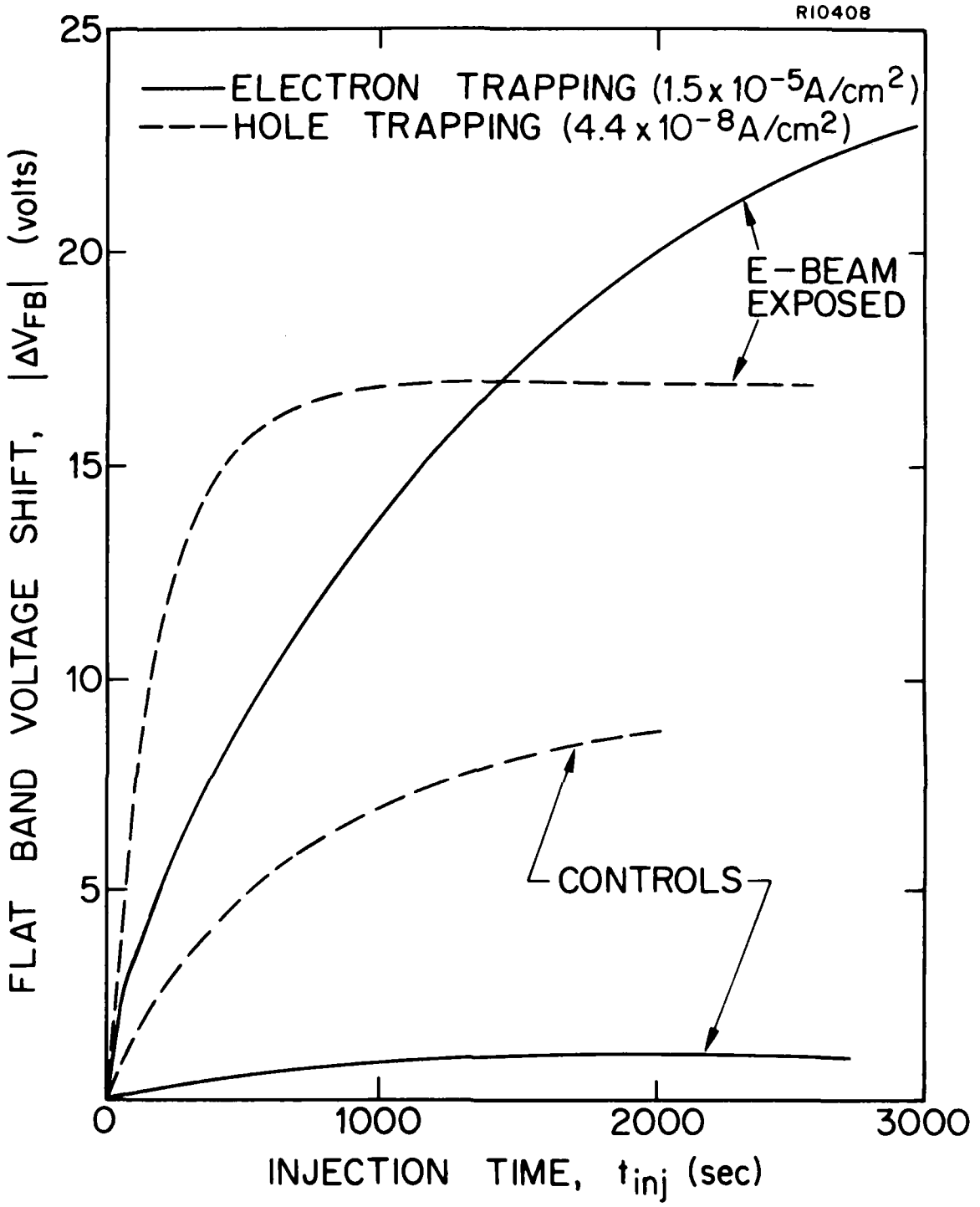

Fig. 4-29. Flat band voltage shift versus injection time for MOS structures on n- and p-type (111) silicon. The structures were exposed to an electron beam fluence of 3.1×10^{-2} C/cm^2 prior to metallization and anneal in forming gas. Control wafers were processed simultaneously but were not exposed to the electron beam.

Raster scanning was accomplished by moving in the x-direction at 2.0 cm sec^{-1} and stepping in the y-direction by 20 μm. Under these conditions, the incident power density was 0.82 MW cm^{-2}, and the calculated antireflective effect of the 800 Å thick oxide was 8%.

Refractive index measurements of the oxide, before and after anneal, did not reveal any change in n to ±0.0005 indicating that the integrity of the oxide was not affected.

The oxides exposed to scanned cw laser beam anneal showed minimum increases in oxide charge densities. Residual fixed oxide charge and interface trapped charge densities following a post-irradiation anneal were less than $3 \times 10^{11}/cm^2$ and $3 \times 10^{10}/cm^2$-eV (at midgap), respectively. Electron and hole trapping by avalanche injection at charge fluxes identical in all parts of this investigation, resulted in minimal increases in flat band voltage shift thereby indicating that laser beam exposure does not generate additional trapping sites.

4.7.4 Exposure to Ion Implantation

Ion implantation through thermally grown SiO_2 films on silicon substrates is known to cause damage to the thermal SiO_2 film. This damage can result, even following a thermal anneal, in increased carrier trapping in the oxide. In this section, however, we investigate implantation into the bare silicon wafer and subsequent oxidation at various temperatures. The goal is to determine whether damage in the silicon substrate itself will result in increased carrier trapping in a subsequently grown oxide.

N-type (100) and (111) silicon wafers were used for this experiment. Following a phosphorus implant at 200 keV with a dose of $10^{13}/cm^2$, the wafers were oxidized along with the control samples at 800°, 900°, 1000°, and 1100°C. Oxide growth was kept at 500 Å instead of the standard 800 Å used in most of this report. This is to compare more directly with the thinner oxide films presently in use in integrated circuit fabrication and to maximize any effects caused by the implantation by reducing the oxidation time and the time for damage anneal.

Results are summarized in Fig. 4-30 and indicate that at all temperatures and for both orientations, ion implantation has led to increased hole trapping. The orientation effect is again consistent with previous results. The flat band voltage shifts obtained are smaller than for similar processed samples in Figs. 4-2 and 4-3 due to the thinner oxide used. This oxide thickness dependence is in agreement with many reports in the literature (37,54,55).

The ion implantation effect observed in Fig. 4-30 is somewhat unexpected, particularly at the higher oxidation temperatures where implantation damage is expected to be annealed out rapidly. These results imply a greater sensitivity to the ion implantation than previously suspected and further work is needed to better understand this effect.

4.8 Relationship between N_{ot} and Other Oxide Charges

The process dependence of N_{ot} outlined in the various preceding sections such as the temperature dependence, anneal ambient dependence, and orientation dependence lead to the interesting question of a possible relationship between N_{ot} and the other oxide charges, primarily N_f and N_{it}. It is well known that both N_f and N_{it} are process dependent and

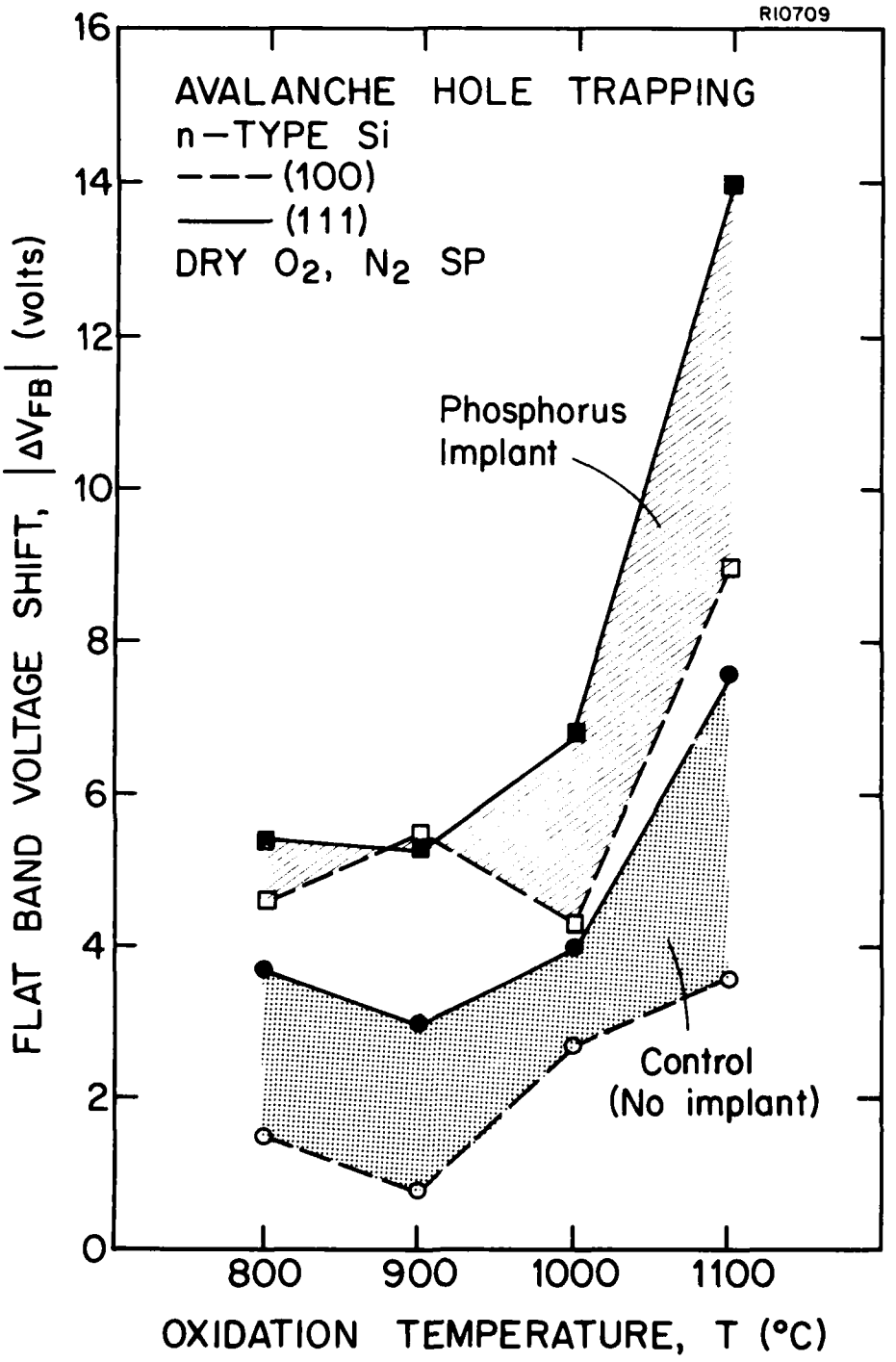

Fig. 4-30. Effect of phosphorus ion implantation on hole trapping in 500 Å thermal oxides.

often in the same fashion. The possible relationship between pre-avalanche charge densities (N_f and N_{it}) and the post-avalanche injection flat band voltage (or N_{ot}) is the subject of this section.

Flat band voltage shifts due to electron and hole trapping are shown in Figs. 4-31 and 4-32 for the case of oxidation in dry O_2 and H_2O followed by post-oxidation in-situ anneal in argon. Also plotted in Fig. 4-31 is the fixed oxide charge density obtained for these samples prior to avalanche charge injection. The general trend for fixed oxide charge N_f is to decrease with increasing oxidation temperature. This is opposite to the hole trapping data but somewhat similar to the electron trapping results. A similar behavior can be seen in Fig. 4-32 for interface trapped charge density at midgap. Both figures suggest that it is unlikely that a relationship exists between N_f prior to avalanche injection and $|\Delta V_{FB}|$ or N_{ot} following avalanche injection.

To further analyze the data, N_f and D_{it} at midgap were plotted versus flat band voltage shifts for all (100) and (111) oriented silicon samples oxidized in dry O_2 and pyrogenic steam and given various post-oxidation anneals. Results for electron trapping are shown in Figs. 4-33(a) and (b)--while hole trapping results are shown in Figs. 4-33(c) and (d). No clear dependence can be observed. A more thorough statistical analysis is required to deconvolute any relationship that may exist. It is clear that further work in this area is necessary.

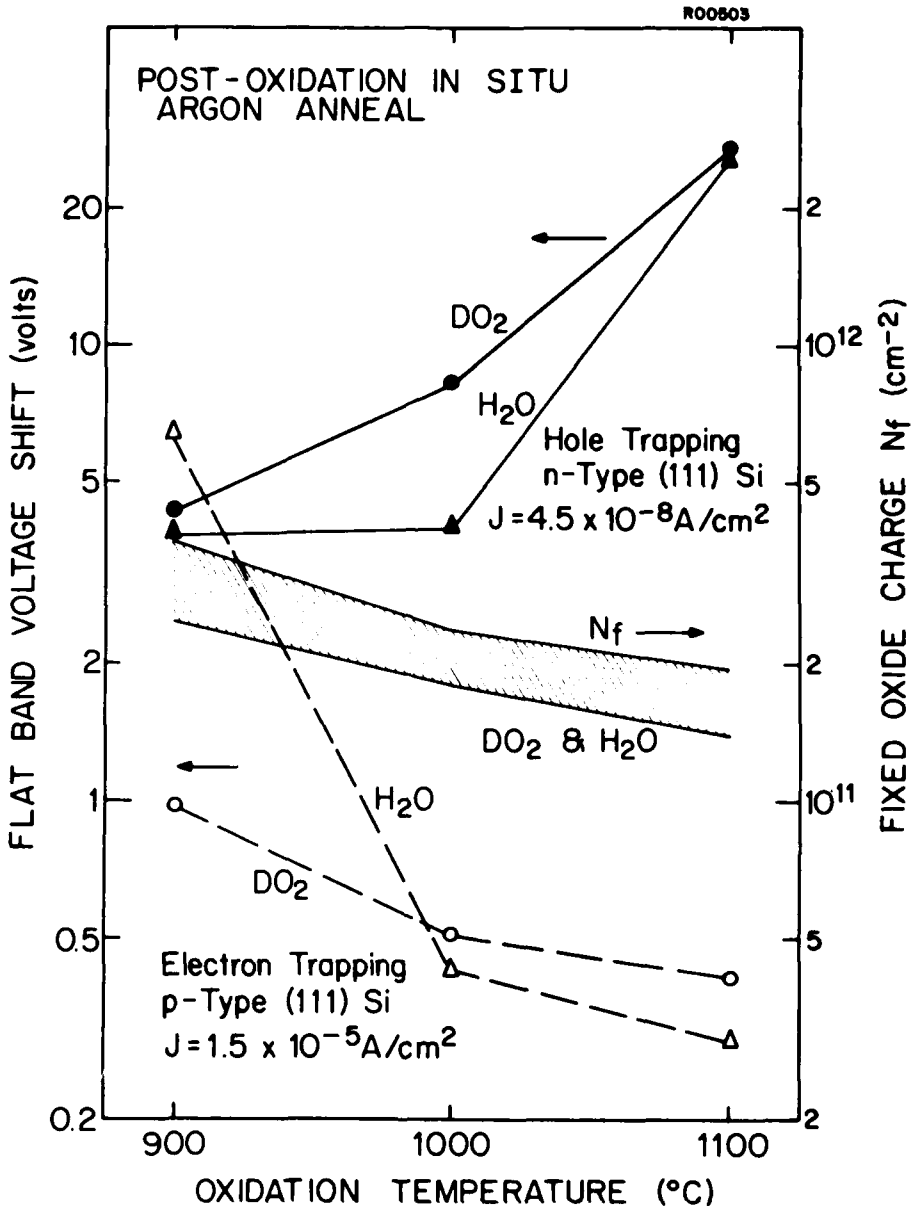

Fig. 4-31. Flat band voltage shift due to avalanche injection and trapping of electrons and holes (left axis) and fixed oxide charge density (right axis) versus oxidation temperature for n- and p-type (111) silicon wafers. Oxidations were carried out in dry O_2 or pyrogenic steam followed by a 10 min anneal in argon and a 2 min pull in argon. Flat band voltage shifts are for 2000 sec injection time at the specified current density.

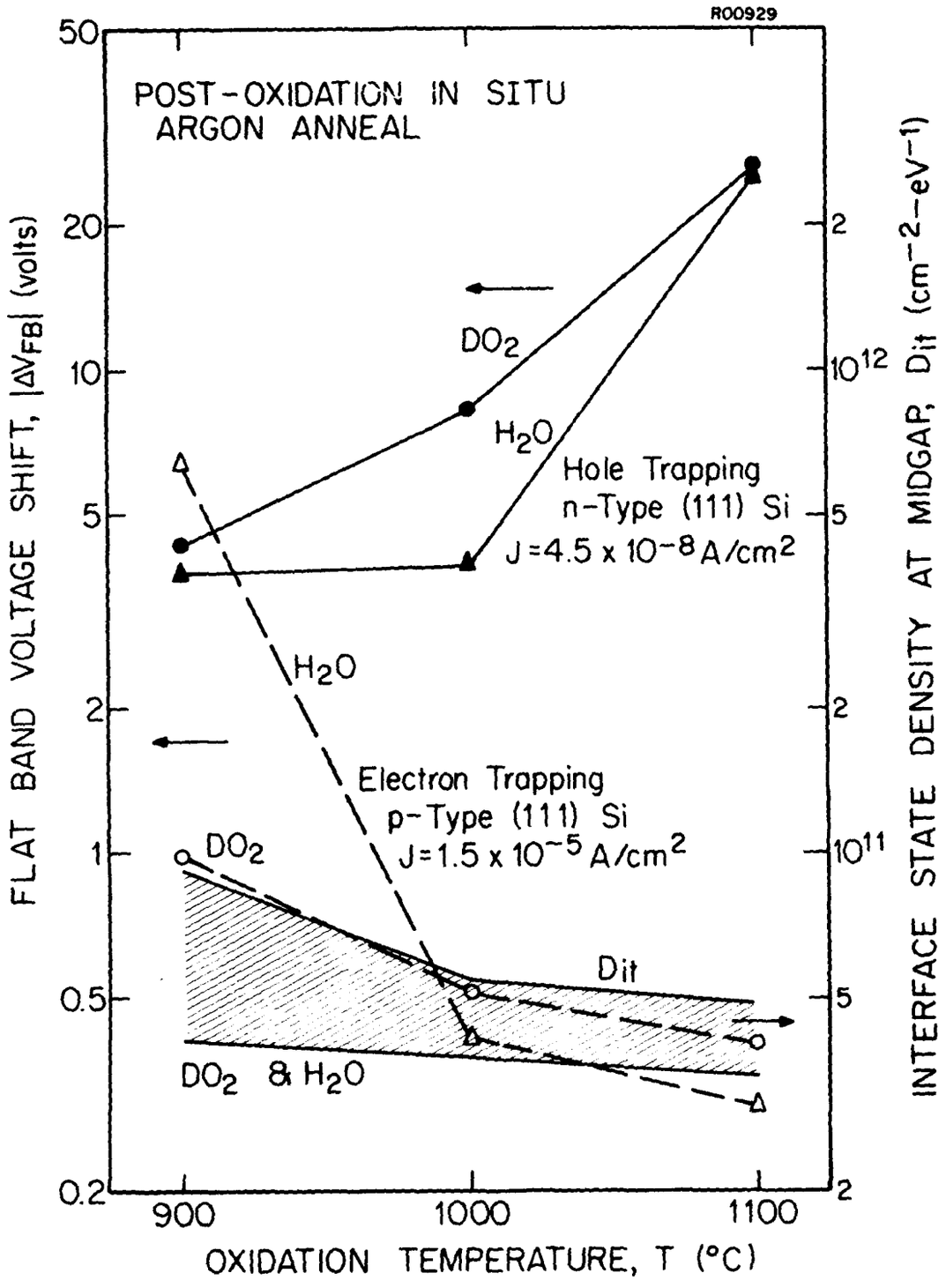

Fig. 4-32. Flat band voltage shift due to avalanche injection and trapping of electrons and holes (left axis) and interface state density at midgap (right axis) versus oxidation temperature for n- and p-type (111) silicon wafers. Other process conditions are the same as Fig. 4-31.

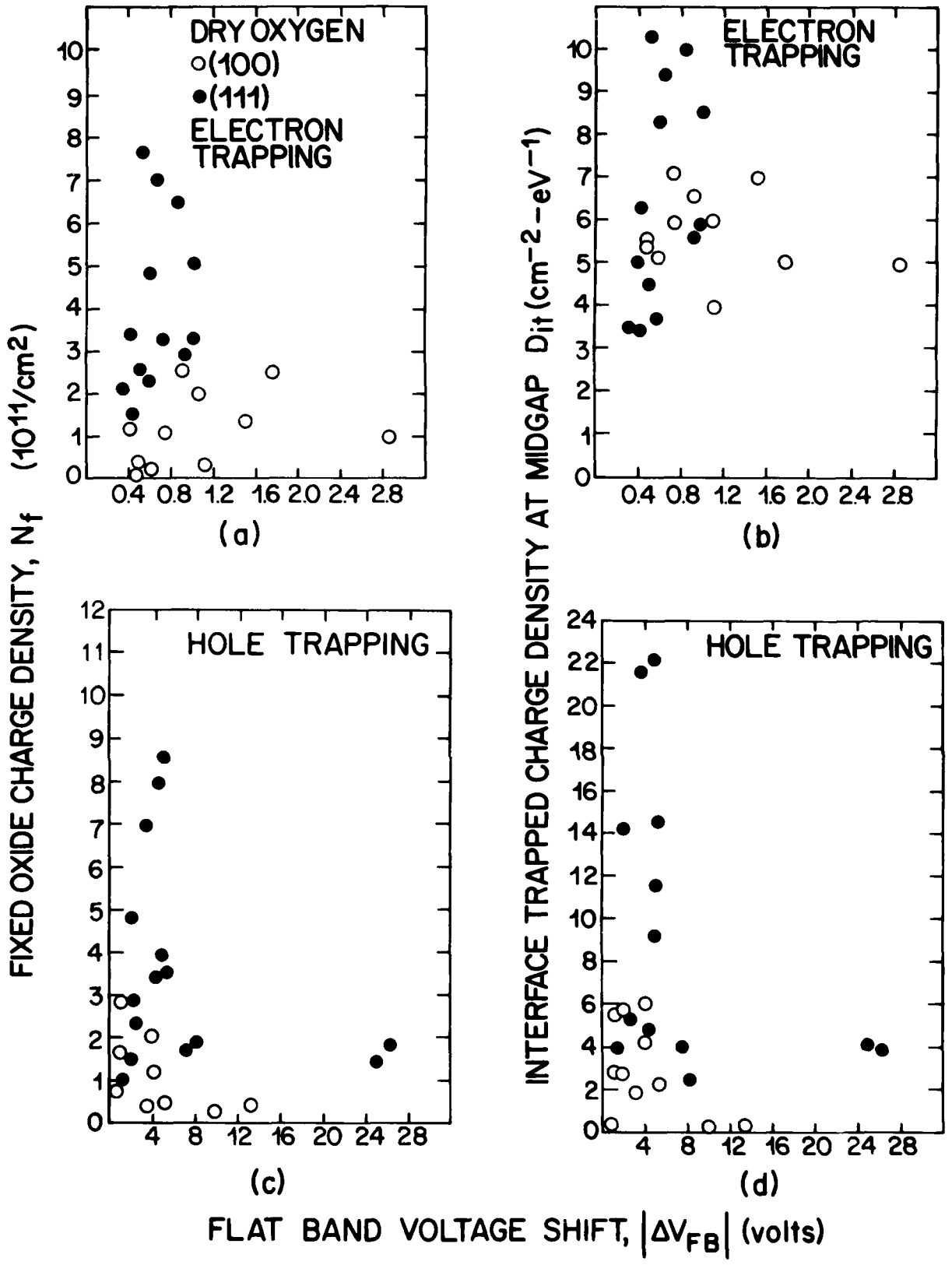

Fig. 4-33. Fixed oxide charge density and interface state density versus flat band voltage shift due to avalanche injection of electrons and holes in oxides grown in dry O_2.

4.9 Radiation Induced Trapped Charge--Process Dependence

One of the main objectives of this program is the characterization of the interrelationship between avalanche injected charge trapping and radiation induced charge trapping. This objective was carried out by sending samples processed simultaneously with the avalanche injection samples to Dr. H. L. Hughes at the Naval Research Laboratory. The wafers were exposed to 1×10^6 rads (Si) under a positive bias of 10 volts. The process dependence of radiation induced trapped charge as measured by Dr. Hughes is discussed in this section. The next section compares the avalanche injection induced charge trapping with the radiation induced charge trapping.

A summary of all flat band voltage shifts obtained at NRL is shown in Tables I and II for oxidations in dry O_2, pyrogenic steam and O_2/HCl. Various plots resulting from these data are presented and compared to the results obtained by avalanche injection.

The radiation exposure results for (100) and (111) n-type Si oxidized in dry O_2 are shown in Fig. 4-34 and indicate that:

1 – The increase in charge trapping for nitrogen and argon anneals at 1100°C is evident. This compares with a similar increase observed in hole injection by avalanche shown in Fig. 4-3.

2 – The orientation dependence previously reported is observed with (100) oriented substrates yielding the lower flat band voltage shift.

TABLE I

Process Parameters and Flat Band Voltage Shifts for n- and p-Type (111) Oxidized Silicon Substrates (NRL)

RUN NO.	WAFER TYPE	OXIDATION AMBIENT	OXIDATION TEMP (°C)	POST-OX ANNEAL AMBIENT*	COOLING AMBIENT	PULL CONDITION	$-\Delta V_{FB}$(volts)** N TYPE H_2	N TYPE N_2	$-\Delta V_{FB}$(volts)** P TYPE H_2	P TYPE N_2
							volts	volts	volts	volts
TR1/TR21	N(111)/P(111)	DRY O_2	900	–	O_2	1-3 sec	1.32 ± .08	1.57 ± .11	4.32 ± .26	4.28 ± .34
TR2/TR22	N(111)/P(111)	DRY O_2	900	–	O_2	10 min	1.27 ± .12	1.40 ± .05	3.27 ± .65	5.23 ± .32
TR3/TR23	N(111)/P(111)	DRY O_2	900	N_2	N_2	2 min	1.12 ± .03	1.45 ± .03	3.58 ± .32	3.87 ± .48
TR4/TR24	N(111)/P(111)	DRY O_2	900	Ar	Ar	2 min	1.08 ± .08	1.37 ± .06	5.57 ±1.51	4.05 ± .35
TR5/TR17	N(111)/P(111)	DRY O_2	1000	–	O_2	1-3 sec	1.27 ± .23	1.33 ± .12	6.60 ± 0	3.22 ± .63
TR6/TR18	N(111)/P(111)	DRY O_2	1000	–	O_2	10 min	1.83 ± .15	1.80 ± .35	3.38 ±1.59	6.70 ± .21
TR7/TR19	N(111)/P(111)	DRY O_2	1000	N_2	N_2	2 min	6.15 ± .64	6.55 ± .05	7.97 ± .06	8.27 ± .58
TR8/TR20	N(111)/P(111)	DRY O_2	1000	Ar	Ar	2 min	5.42 ± .56	4.80 ± .31	6.90 ± .26	7.33 ± .50
TR 9/TR13	N(111)/P(111)	DRY O_2	1100	–	O_2	1-3 sec	2.27 ± .06	2.17 ± .06	3.75 ± 0	3.97 ± .11
TR10/TR14	N(111)/P(111)	DRY O_2	1100	–	O_2	10 min	1.58 ± .04	1.97 ± .57	2.69 ± .38	4.2 ± .22
TR11/TR15	N(111)/P(111)	DRY O_2	1100	N_2	N_2	2 min	28.5 ± .7	31.2 ± .8	30.9 ± 1.0	21.3 ± .95
TR12/TR16	N(111)/P(111)	DRY O_2	1100	Ar	Ar	2 min	29.8 ± .9	30.2 ± 1.0	26.9 ± 1.0	31.3 ± 1.0
TR25/TR40	N(111)/P(111)	PYROGENIC STEAM	900	–	STEAM	1-3 sec	7.43 ± 1.4	4.27 ± 1.2	8.7 ± .6	10.8 ± 2.5
TR26/TR41	N(111)/P(111)	PYROGENIC STEAM	900	N_2	N_2	2 min	2.93 ± .21	0.32 ± .03	2.1 ± .5	2.75 ± 1.8
TR27/TR42	N(111)/P(111)	PYROGENIC STEAM	900	Ar	Ar	2 min	1.92 ± .6	1.51 ± 1.0	16.0 ± .5	2.1 ± .1
TR28/TR37	N(111)/P(111)	PYROGENIC STEAM	1000	–	STEAM	1-3 sec	2.6 ± .7	2.4 ± .5	14.0 ± .5	6.0 ± .5
TR29/TR38	N(111)/P(111)	PYROGENIC STEAM	1000	N_2	N_2	2 min	3.7 ± .2	4.5 ± .2	22.8 ± .4	9.4 ± .1
TR30/TR39	N(111)/P(111)	PYROGENIC STEAM	1000	Ar	Ar	2 min	2.7 ± .5	2.9 ± .2	13.0 ± .6	4.7 ± .1
TR31/TR34	N(111)/P(111)	PYROGENIC STEAM	1100	–	STEAM	1-3 sec	2.1 ± .5	1.8 ± .2	3.2 ± .03	4.0 ± .4
TR32/TR35	N(111)/P(111)	PYROGENIC STEAM	1100	N_2	N_2	2 min	35.5 ± .3	31.1 ± 1.5	–	>-70
TR33/TR36	N(111)/P(111)	PYROGENIC STEAM	1100	Ar	Ar	2 min	34.8 ± 1.2	32.6 ± 1.8	-66.0 ± .9	-66.9 ± .4
TR43/TR46	N(111)/P(111)	O_2HCl	1000	Ar	Ar	2 min	12.4 ± .1	12.6 ± .2	17.4 ± .1	16.6 ± .5
TR44/TR46	N(111)/P(111)	O_2HCl	1000	N_2	N_2	2 min	11.3 ± .4	11.9 ± .4	16.3 ± .7	18.6 ± .4

*ANNEAL IS IN SITU FOR 10 MINUTES AT GROWTH TEMPERATURE

**FOR IRRADIATION BIAS STRESS OF 10^6rads AT +10 volts

TABLE II

Process Parameters and Flat Band Voltage Shifts for n- and p-Type (100) Oxidized Silicon Substrates (NRL)

RUN NUMBER		WAFER TYPE		OXIDATION		POST-OX ANNEAL AMBIENT*	PULL CONDITION GAS/TIME	$-\Delta V_{FB}$ (volts)**			
								N-TYPE		P-TYPE	
N-TYPE	P-TYPE			AMBIENT	TEMP			H_2	N_2	H_2 *	N_2
TR-101	TR-113	N(100)	P(100)	DRY O_2	900°C		O_2 1-3 sec	1.7 ± .4	1.0 ± 0	24.4 ± 1.7	2.3 ± .3
102	114	N(100)	P(100)	DRY O_2	900°C	–	O_2 10 min	3.6 ± .3	0.97 ± .2	30.8 ± 1.6	2.5 ± .1
103	115	N(100)	P(100)	DRY O_2	900°C	N_2	N_2 2 min	5.3 ± .2	3.6 ± .4	26.7 ± .8	2.6 ± .1
104	116	N(100)	P(100)	DRY O_2	900°C	Ar	Ar 2 min	3.9 ± .4	1.2 ± .5	25.2 ± .3	1.8 ± 0
105	117	N(100)	P(100)	DRY O_2	1000°C	–	O_2 1-3 sec	0.73 ± .21	1.03 ± .06	23.5 ± .2	1.2 ± .1
106	118	N(100)	P(100)	DRY O_2	1000 C	–	O_2 10 min	3.7 ± .5	3.1 ± .04	22.5 ± .6	1.5 ± 0
107	119	N(100)	P(100)	DRY O_2	1000°C	N_2	N_2 2 min	2.95 ± 0.4	5.3 ± 0	23.5 ± .6	7.2 ± .1
108	120	N(100)	P(100)	DRY O_2	1000°C	Ar	Ar 2 min	3.9 ± 0.8	3.1 ± .1	22.1 ± 4.9	5.6 ± .4
109	121	N(100)	P(100)	DRY O_2	1100°C	–	O_2 1-3 sec	1.6 ± .1	1.5 ± .5	9.6 ± 1.1	3.8 ± .1
110	122	N(100)	P(100)	DRY O_2	1100°C	–	O_2 10 min	4.8 ± .3	1.2 ± .1	21.2 ± 2.1	2.9 ± .2
111	123	N(100)	P(100)	DRY O_2	1100°C	N_2	N_2 2 min	13.4 ± 2.3	22.4 ±3.3	32.0 ± .4	29.2 ± .2
112	124	N(100)	P(100)	DRY O_2	1100°C	Ar	Ar 2 min	8.2 ± .9	15.0 ± .8	32.0 ± .5	18.5 ±1.0
125	134	N(100)	P(100)	PYROGENIC STEAM	900°C	–	STEAM 1-3 sec	3.7 ± 1.0	1.2 ± .2	25.4 ± 0	7.2 ± .3
126	135	N(100)	P(100)	PYROGENIC STEAM	900°C	N_2	N_2 2 min	2.3 ± .5	0.2 ± .08	20.3 ± .3	6.4 ±1.5
127	136	N(100)	P(100)	PYROGENIC STEAM	900°C	Ar	Ar 2 min	1.3 ± 1.6	0.1 ± 0	27.5 ±10	3.0 ± .2
128	137	N(100)	P(100)	PYROGENIC STEAM	1000°C	–	STEAM 1-3 sec	3.0 ± .2	1.2 ± .2	–	3.8 ± .1
129	138	N(100)	P(100)	PYROGENIC STEAM	1000°C	N_2	N_2 2 min	9.3 ± 2.0	2.2 ± 0	17.9 ± 1.8	4.0 ± 0
130	139	N(100)	P(100)	PYROGENIC STEAM	1000°C	Ar	Ar 2 min	6.3 ± 1.1	2.4 ± .1	16.6 ± .3	2.8 ± .4
131	140	N(100)	P(100)	PYROGENIC STEAM	1100°C	–	STEAM 1-3 sec	12.0 ± .3	4.8 ± .5	21.9 ± .4	5.6 ±1.0
132	141	N(100)	P(100)	PYROGENIC STEAM	1100°C	N_2	N_2 2 min	16.1 ± 3.4	20.8 ± .4	28.5 ± 0	21.5 ± .1
133	142	N(100)	P(100)	PYROGENIC STEAM	1100°C	Ar	Ar 2 min	11.5 ± 1.4	13.2 ± .6	22.7 ± .3	15.8 ± .7

H_2 = PRE METALLIZATION ANNEAL: 400 C, 20 min IN H_2

N_2 = POST METALLIZATION ANNEAL: 400 C, 20 min IN F G.

* = ANNEAL IN SITU FOR 10 min AT GROWTH TEMPERATURE

** = FOR IRRADIATION BIAS STRESS OF 10^6 rads, +10v

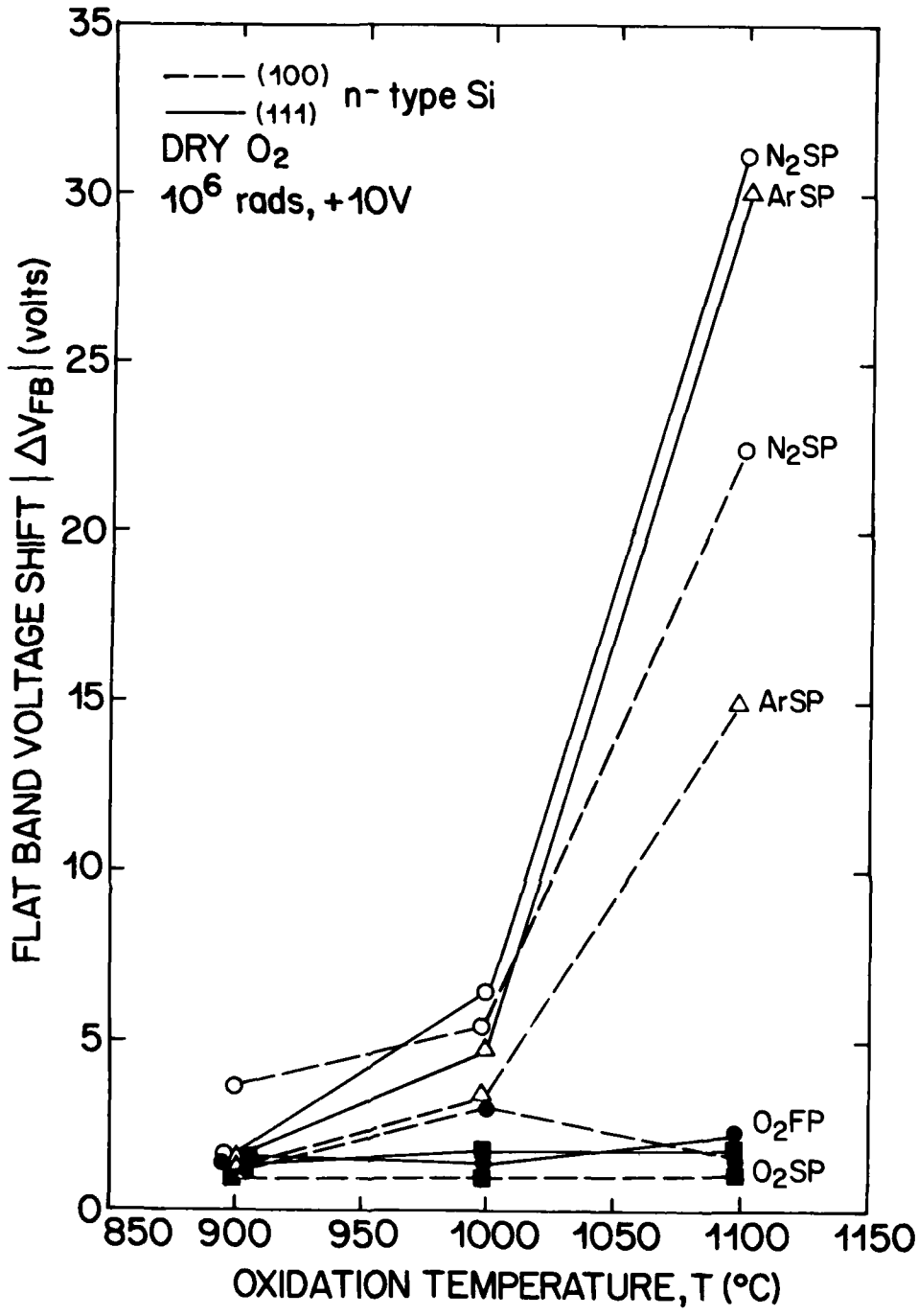

Fig. 4-34. Change in flat band voltage following irradiation versus oxidation temperature for trapping from n-type (100) and (111) substrates. Samples were oxidized in dry O_2 and received a post-metallization anneal at 400°C in 10% H_2 in N_2 for 10 min. Irradiation parameters: 10^6 rads, +10 V.

3 – Cooling in the oxidizing ambient O_2FP and O_2SP results in small variation in charge trapping with oxidation temperature. This effect was also observed in avalanche injected hole trapping.

It should be noted that in the case of exposure to ionizing radiation, the substrate material does not play a critical role and the dominant trapping mechanism observed is that of hole trapping. This behavior is illustrated in Fig. 4-35 and holds for most measurements, the exception being for p-type (100) wafers exposed to a pre-metallization anneal in hydrogen. In this case, the results appear to indicate enhanced hole trapping for p-type substrates. A clear explanation is not available at this time and only further experimentation can clarify this point.

Radiation exposure results for (100) and (111) n-type Si oxidized in steam are shown in Fig. 4-36 and can be compared directly to the avalanche results in Fig. 4-7. The only obvious difference is that the wafers pulled in the steam ambient result in more charge trapping when carriers are avalanche injected than when the carriers are radiation induced. This may be due to increased interface trap generation during avalanche injection through a hydrogen-rich interface resulting from the quench in steam.

The effect of post-metallization anneal in 10% hydrogen in nitrogen forming gas or 100% N_2 is shown in Fig. 4-37. The results indicate no major differences, again in agreement with the avalanche injection results of Fig. 4-16.

In summary, many of the processing dependence results observed for radiation induced trapping are similar to those for avalanche injection trapping. The only obvious deviation

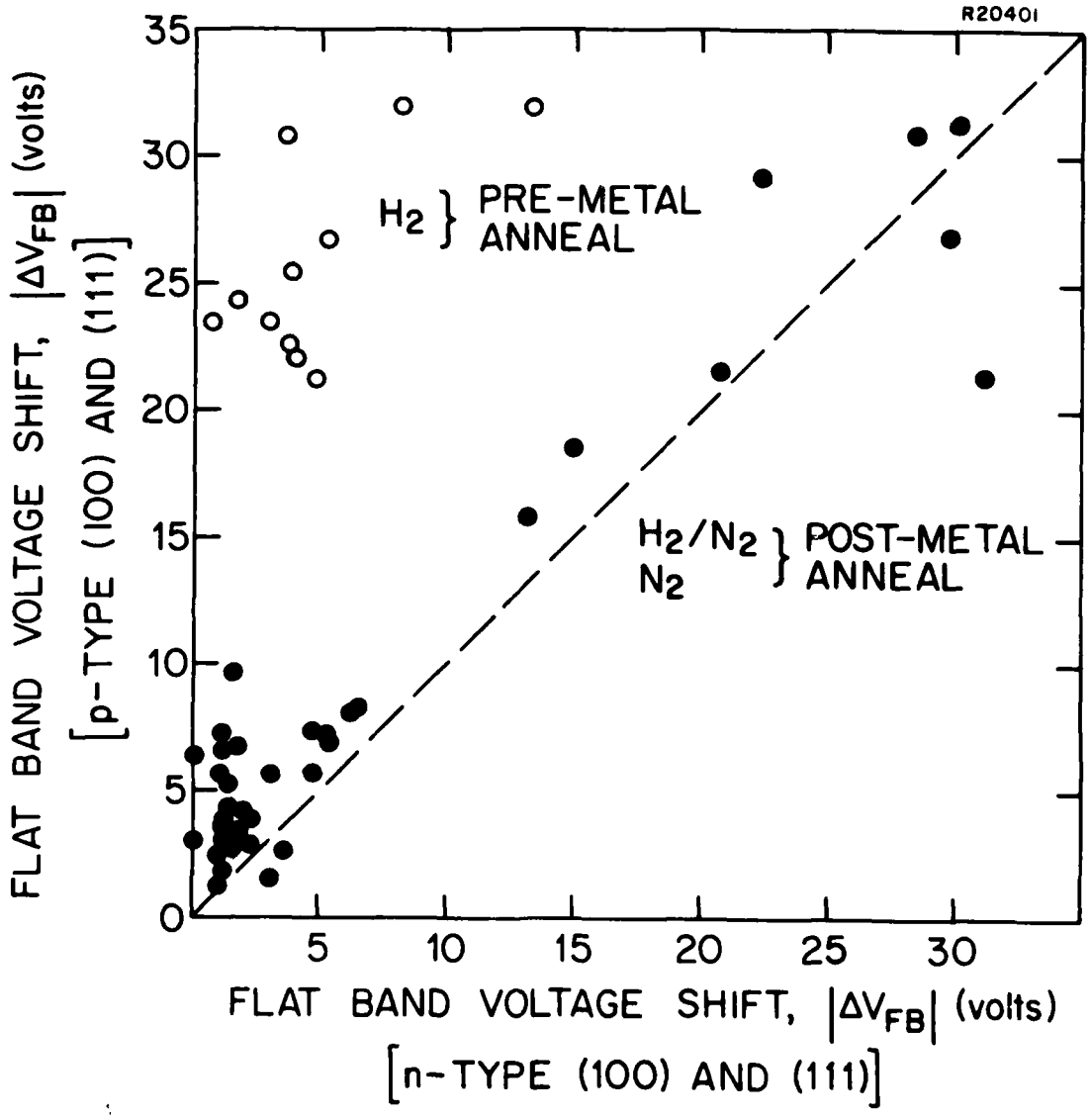

Fig. 4-35. Flat band voltage shift for n-type (100) and (111) MOS structures versus flat band voltage for p-type (100) and (111) structures. Dry and steam oxidation. Note result for 100% H_2 pre-metallization anneal.

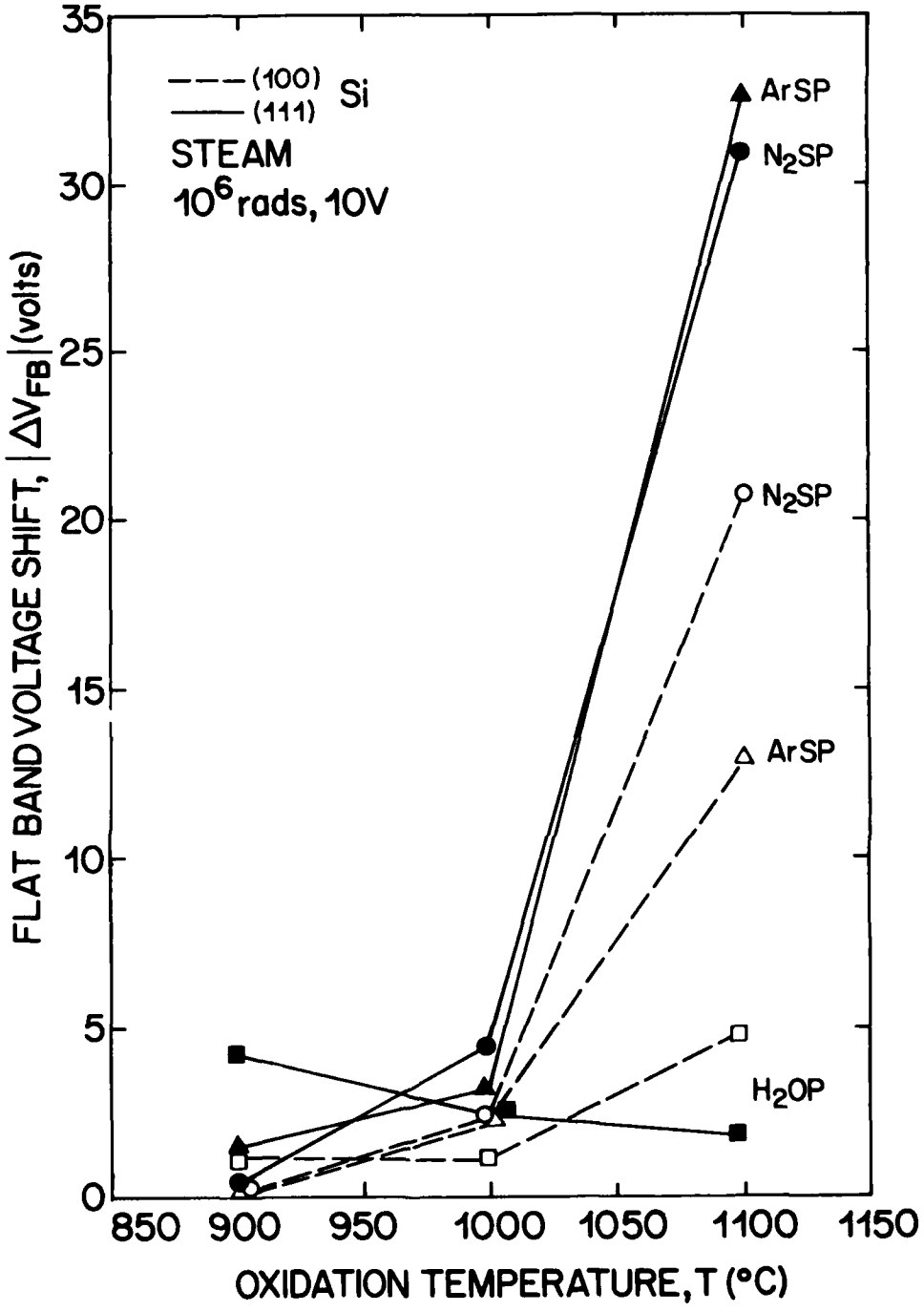

Fig. 4-36. Flat band voltage shift following irradiation versus steam oxidation temperature for trapping from n-type (100) and (111) substrates. Other process conditions are the same as Fig. 4-34.

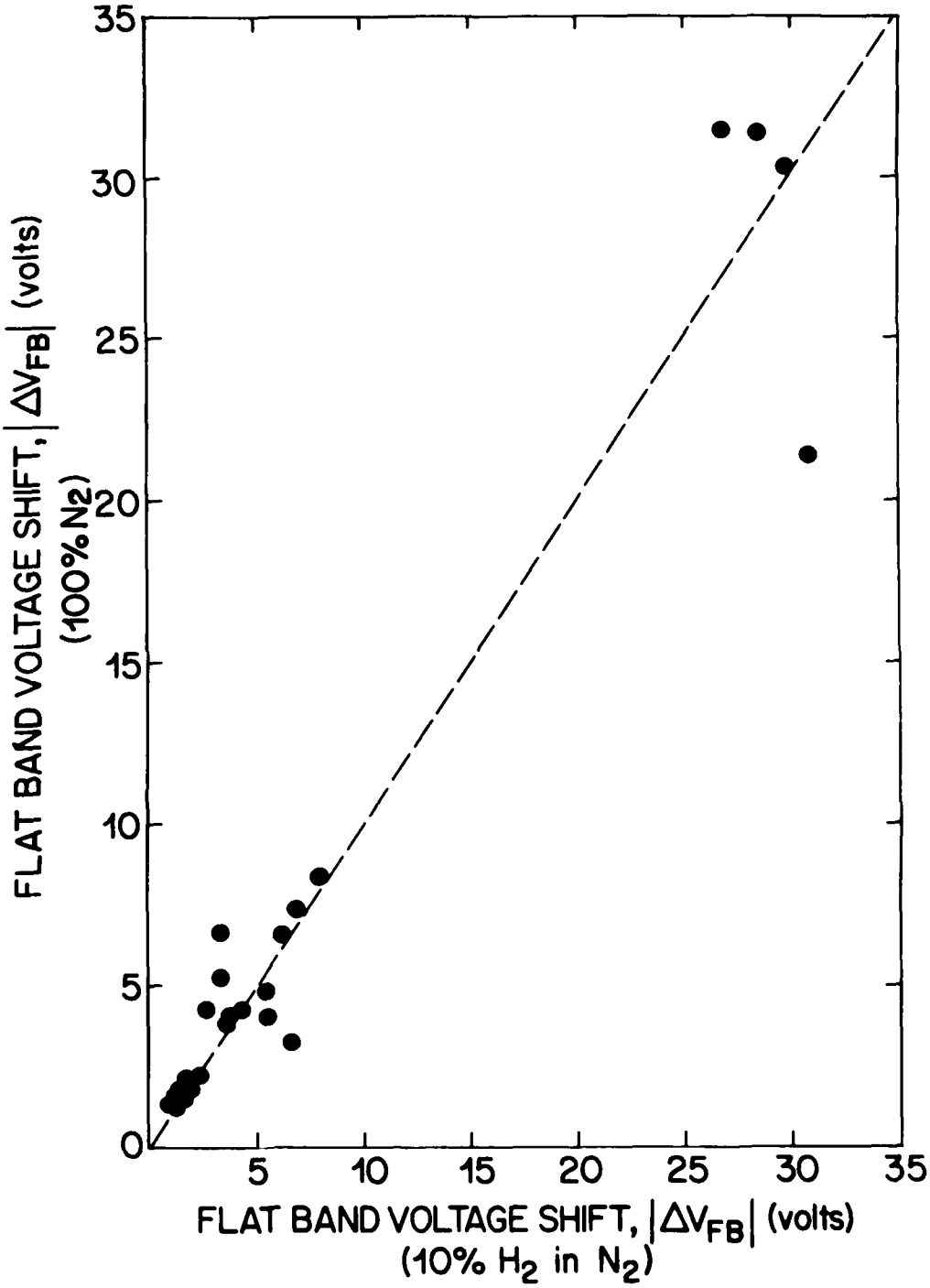

Fig. 4-37. Flat band voltage shift resulting from irradiation of MOS structures that received a 10% H_2 in N_2 post-metallization anneal versus MOS structures that received a 100% N_2 anneal.

occurs for radiation induced charge trapping on p-type (100) substrates annealed prior to metallization in hydrogen. These results are considered in question in this report and will need further verification.

4.10 Relationship between Radiation Induced and Avalanche Injected Carrier Trapping

The processing dependences of radiation induced carrier trapping presented in Figs. 4-34 and 4-36 and the obvious similarity to results obtained for hole trapping by avalanche injection suggest that for hole trapping in thermal oxides a relationship exists between the two carrier trapping processes. In order to highlight such a relationship further, all flat band voltage shifts resulting from radiation induced charge trapping in dry O_2 oxides were plotted in Fig. 4-38 versus the corresponding shift obtained from avalanche charge injection measurement at 2000 sec for a current density of 4.4×10^{-8} A/cm^2. Although there is substantial scatter, it is clear that some relationship exists. The results for (100) oriented substrates are different than the results for (111) substrates, indicating that radiation testing may be more sensitive to process variations on (100) substrates than on (111) substrates. It should be pointed out that the data could be expanded by varying the radiation dose or the injected carrier density.

A similar plot for steam grown oxides is shown in Fig. 4-39. One striking feature of this plot is the reduced carrier trapping apparent in the radiation test. This result is however quite deceiving and can be easily understood by recalling that generation of interface states in steam oxides results in a reduction in flat band voltage. This reduction is a strong function of the injected carrier density. The

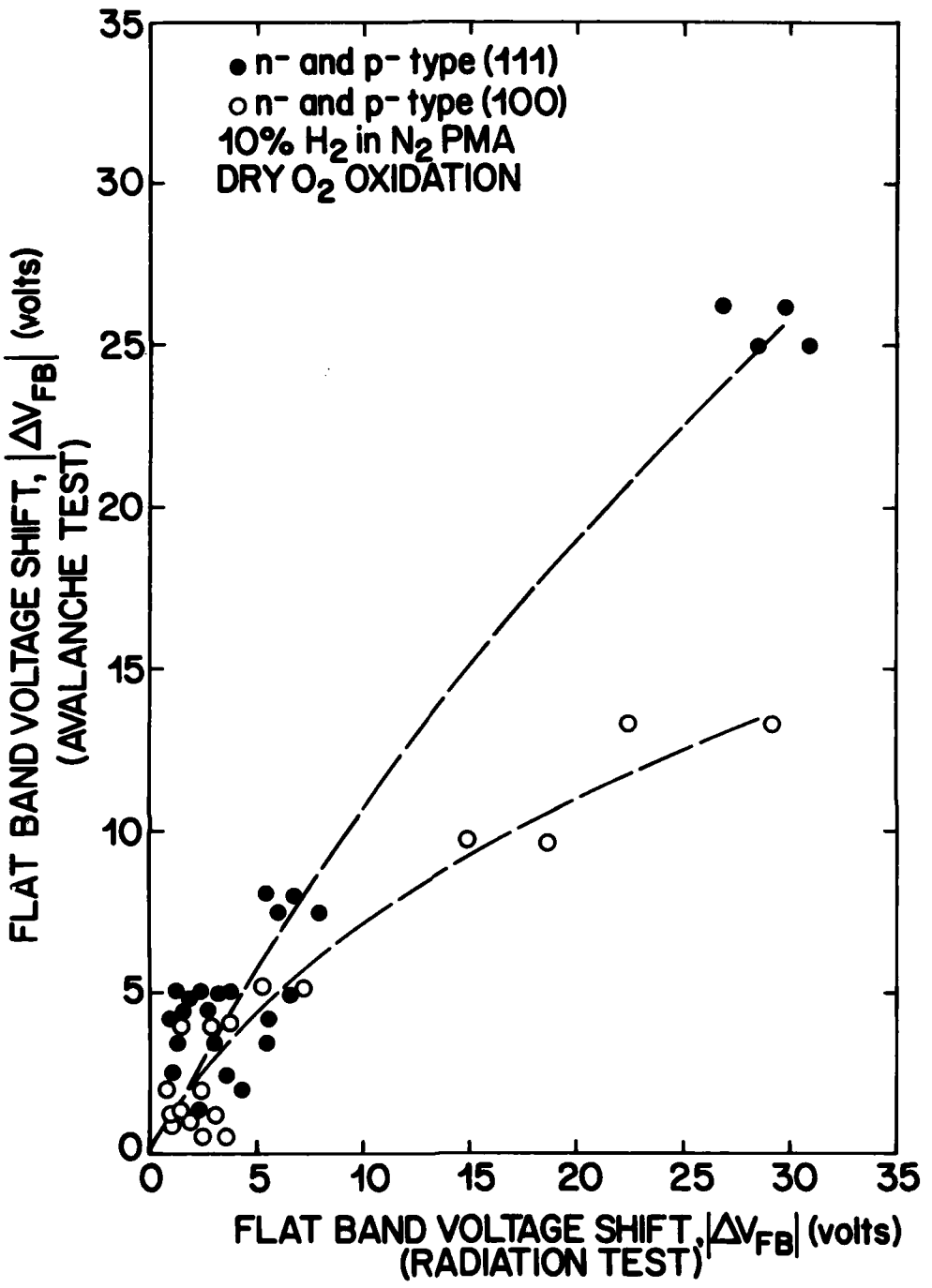

Fig. 4-38. Flat band voltage shift following 2000 sec of injection time versus flat band voltage shift due to radiation exposure. Oxides were grown in dry O_2.

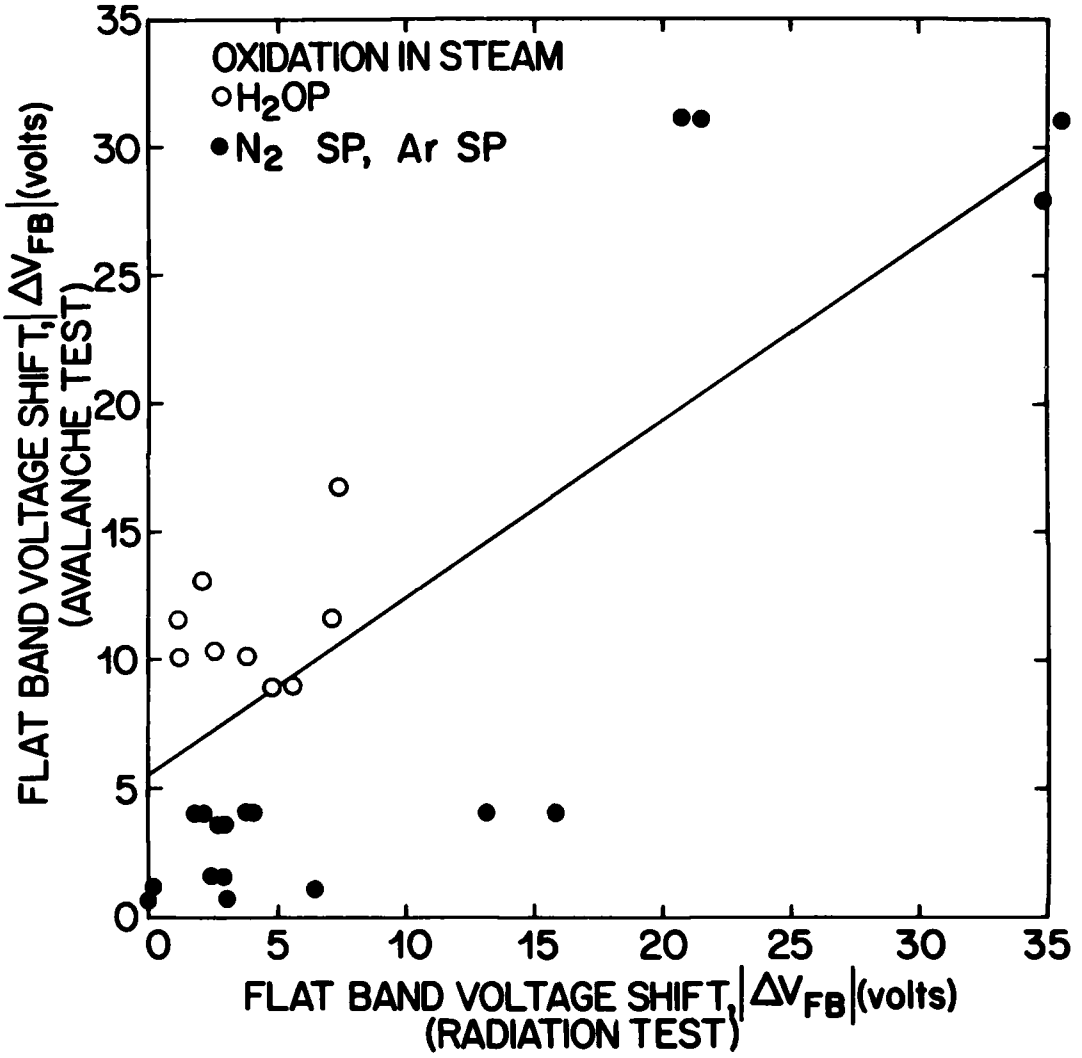

Fig. 4-39. Flat band voltage shift following 2000 sec of injection time versus flat band voltage shift due to radiation exposure. Oxides were grown in pyrogenic steam.

dose used in the radiation testing could be high enough to generate sufficient interface trapped charges to reduce the flat band voltage shift in the manner illustrated in Fig. 4-9. In summary, when the data resulting from the steam oxidation and cool (H_2OP) are examined carefully it is evident that the overwhelming majority of the data indicate a strong correlation between avalanche injected carrier trapping and radiation induced carrier trapping.

These results lead to three major conclusions:

(a) The traps present in the oxide and populated by avalanche injection or radiation exposure are strongly process dependent.

(b) The density of carriers trapped is dependent on the technique used to populate the traps. Except for the differing rates of interface trap generation during the testing, a relationship is evident between flat band voltage shifts given by the different test methods. This suggests that the trap density measured is largely independent of the method by which the carriers are injected, be it ionizing radiation or injection over the barrier due to avalanche.

(c) Due to this relationship between radiation induced charge trapping and avalanche injected charge trapping, testing for radiation sensitivity can be carried out by avalanche injection rather than radiation exposure, therefore allowing for the possibility of on-chip radiation hardness testing. This last result could have significant implications in improving the reliability of radiation sensitive devices.

5.0 SUMMARY

The effects of processing variables on the trapping characteristics of injected charge carriers in thermal silicon dioxide have been characterized for a large variety of typical IC fabrication processing steps. The process dependence of the trapped charge was compared to those produced by exposure to ionizing radiation. The results show a definite correlation between the two methods of carrier generation and trapping, suggesting that avalanche carrier injection could be used as a quick routine on-chip test for the radiation sensitivity of a given process or processing sequence.

5.1 Optimum Process Parameters for Minimum Radiation Sensitivity

In order to summarize some of the findings from this report, it is interesting to consider the fabrication of a hypothetical device containing both n- and p-channel devices, with the major requirement being minimum charge trapping in the gate oxide. Such a device could be fabricated according to the following rules:

(a) The substrate used should have (100) orientation to minimize all oxide charges.

(b) The oxidation can be carried out in dry O_2 or steam at 1 atm if followed by a nitrogen anneal at 900°C (possibly at 1000°C). High pressure steam would result in increased electron trapping.

(c) Poly-Si gates or fieldplates may lead to erratic results but the conditions of growth of the underlying oxide are generally dominant.

(d) Exposure to pure hydrogen for low temperature anneals should be minimized. Aluminum post-metallization anneal should be used when possible.

(e) Ion implantation will result in some degradation even when oxide is grown following implant. For annealing implant damage with minimum dopant redistribution, a laser anneal (topside) or electron beam anneal (backside) is recommended for minimum effect on oxide sensitivity to trapped charges.

6.0 FUTURE WORK

The primary objective of this program was, and will continue to be, to obtain a better understanding of the process dependence of charge trapping in thermal oxides. To accomplish this objective, the dependence of both electron and hole trapping on some process variables involved in the oxide preparation was determined in the first two years of the program. Furthermore, charge trapping induced by avalanche injection was related to that induced by ionizing radiation. Data gathered as part of this program have already yielded a substantial amount of information that can be used in the optimization of the process variables that will lead to minimum charge trapping in VLSI device structures. The relationship observed between avalanche injection trapping and ionizing radiation trapping will be used to develop an accelerated test procedure, involving test structures compatible with current and projected VLSI device processing, which would allow on-chip testing for radiation sensitivity.

Future work under this program can be divided into two areas. The first area is aimed at extending the process dependence data obtained and covering new areas such as damage due to implants, plasma processing effects, and others. The structures will be tested by avalanche injection as well as ionizing radiation. The second area will deal with the investigation of test structures suitable for incorporation on VLSI wafers and compatible with VLSI processing.

These test structures will be fabricated on high resistivity material (5-18 Ω-cm) typically used for MOS VLSI circuit manufacturing. Oxides grown on such high resistivity material are not suitable for avalanche charge injection and trapping experiments as a result of the high voltages that are required

to generate the fields necessary for impact ionization on the substrate. Ion implantation will therefore be used to increase the dopant levels at the surface of the silicon to the vicinity of 1×10^{17} to $3 \times 10^{17}/cm^3$. It should be noted that preliminary results outlined in Section 4.7.4 show that ion implantation can result in increased charge trapping in thermal oxides. These results also show, however, that the dependence of charge trapping on pre-implantation parameters is not masked by the implantation effects. Based on this finding, oxide sensitivity to radiation induced or avalanche injected charges can be monitored by means of a high resistivity, ion implanted substrate. In this part of the program, test structures with ion implanted regions will be compared to nonimplanted low resistivity structures used in the first two years of the program.

REFERENCES

(1) W. A. Pliskin and R. A. Gdula, in "Handbook of Semiconductors," T. S. Moss, Ed., Vol. 3, S. P. Keller, Ed., North Holland Publishing Co., New York (1980).

(2) R. Champagne and M. Toole, Solid-State Tech. 20, 61 (1977).

(3) B. E. Deal and A. S. Grove, J. Appl. Phys. 36, 3770 (1965).

(4) B. E. Deal, J. Electrochem. Soc. 121, 198C (1974).

(5) B. E. Deal, IEEE Trans. Electron Devices ED-27, 606 (1980).

(6) B. E. Deal, in "Semiconductor Silicon 1977," H. R. Huff and E. Sirtl, Eds., pp. 276-296, The Electrochemical Society, Inc., Princeton, New Jersey (1977).

(7) P. J. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk, J. Appl. Phys. 50, 5847 (1979).

(8) B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, J. Electrochem. Soc. 114, 266

(9) D. R. Lamb and F. R. Badcock, Int. J. Electronics 24, 11 (1968).

(10) F. Montillo and P. Balk, J. Electrochem. Soc. 118, 1463 (1971).

(11) W. M. Werner, J. Electrochem. Soc. 123, 540 (1976).

(12) R. R. Razouk and B. E. Deal, J. Electrochem. Soc. 126, 1573 (1979).

(13) R. Williams, Phys. Rev. 140, A569 (1965).

(14) A. M. Goodman, Phys. Rev. 152, 785 (1966).

(15) A. M. Goodman, J. Appl. Phys. 37, 3580 (1966).

(16) E. H. Nicollian, A. Goetzberger, and C. N. Berglund, Appl. Phys. Lett. 15, 174 (1969).

(17) E. H. Nicollian and C. N. Berglund, J. Appl. Phys. 41, 3052 (1970).

(18) K. Nagai, Y. Hayashi, and Y. Tarui, Jap. J. Appl. Phys. 14, 1539 (1975).

(19) J. F. Verwey, J. Appl. Phys. 44, 2681 (1973).

(20) T. H. Ning and H. N. Yu, J. Appl. Phys. 45, 5373 (1974).

(21) D. R. Young, J. Appl. Phys. 47, 2098 (1976).

(22) R. Williams and M. H. Woods, J. Appl. Phys. 44, 1026 (1973).

(23) E. Harari, S. Wang, and B. S. H. Royce, J. Appl. Phys. 46, 1310 (1975).

(24) R. C. Hughes, Appl. Phys. Lett. 26, 436 (1975).

(25) J. M. Aitken and D. R. Young, J. Appl. Phys. 47, 1196 (1976).

(26) J. L. Peel and R. C. Eden, IEEE Trans. Nucl. Sci. NS-18,

(27) R. J. Powell and G. F. Derbenwick, IEEE Trans. Nucl. Sci. NS-18, 99 (1971).

(28) Z. A. Weinberg, Appl. Phys. Lett. 27, 437 (1975).

(29) R. J. Powell, J. Appl. Phys. 46, 4557 (1975).

(30) A. G. Thomas, S. R. Butler, J. I. Goldstein, and P. D. Parry, IEEE Trans. Nucl. Sci. NS-21, 14 (1974).

(31) R. A. Gdula, Tech. Digest, IEEE International Electron Device Meeting, p. 148 (1977).

(32) T. H. Ning, J. Appl. Phys. 49, 4077 (1978).

(33) R. A. Gdula, J. Electrochem. Soc. 123, 42 (1976).

(34) D. J. Coe, Solid-State Electron Dev. 2, 57 (1978).

(35) K. G. Aubuchon, IEEE Trans. Nucl. Sci. NS-18, 117 (1971).

(36) J. M. Aitken and D. R. Young, IEEE Trans. Nucl. Sci. NS-24, 2128 (1977).

(37) D. R. Young, E. A. Irene, D. J. DiMaria, R. F. DeKeersmaecker, and H. Z. Massoud, J. Appl. Phys. 50, 6366 (1979).

(38) R. R. Razouk, L. N. Lie, and B. E. Deal, J. Electrochem. Soc. 128, 2214 (1981).

(39) D. R. Young, private communication.

(40) D. R. Lamb and F. R. Badcock, Int. J. Electron. 24, 11 (1968).

(41) G. W. Hughes, Final Report No. PRRL-77-CR-5, February 1977, Contract No. N00014-74-C-0185.

(42) H. L. Hughes, IEEE Trans. Nucl. Sci. NS-22, 2118 (1975).

(43) L. N. Lie, R. R. Razouk, and B. E. Deal, submitted for publication.

(44) A. R. Kirkpatrick, J. A. Minnucci, and A. C. Greenwald, IEEE Trans. Electron Devices ED-24, 429 (1977).

(45) A. C. Greenwold, A. R. Kirkpatrick, R. G. Witte, and J. A. Minnucci, J. Appl. Phys. 50, 783 (1979).

(46) T. I. Kamins and P. H. Rose, J. Appl. Phys. 50, 1308 (1979).

(47) A. G. Cullis, H. C. Weber, and N. G. Chew, Appl. Phys. Lett. 36, 547 (1980).

(48) A. Gat and J. F. Gibbons, Appl. Phys. Lett. 32, 142 (1978).

(49) A. Gat and J. F. Gibbons, T. J. Magee, J. Peng, V. R. Deline, P. Williams, and C. A. Evans Jr., Appl. Phys. Lett. 32, 276 (1978).

(50) S. Schiller, S. Panzer, and R. Klabes, Thin Solid Films 73, 221 (1980).

(51) R. A. McMahon and H. Ahmed, Electron. Lett. 15, 45 (1979).

(52) T. O. Yep, R. T. Fulks, and R. A. Powell, Appl. Phys. Lett. 38, 162 (1981).

(53) R. R. Razouk, M. Delfino, R. T. Fulks, R. A. Powell, and T. O. Yep, J. Appl. Phys. 53, 800 (1982).

(54) G. F. Derbenwick and B. L. Gregory, IEEE Trans. Nucl. Sci. NS-22, 2151 (1975).

(55) C. R. Viswanathan and J. Maserjian, IEEE Trans. Nucl. Sci. NS-23, 1540 (1976).